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RELIABILITY ASSESSMENT AND FAULT-TOLERANCE SCHEMES FOR MODULAR MULTILEVEL CONVERTER-BASED STATCOM

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João Victor Matos Farias

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"RELIABILITY ASSESSMENT AND FAULT-TOLERANCE SCHEMES FOR MODULAR MULTILEVEL CONVERTER-BASED STATCOMS"

JOÃO VICTOR MATOS FARIAS

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"Facilmente não existe por aqui
Simplesmente não é assim como se diz..."
CPM 22

Resumo

O cenário atual dos sistemas elétricos de potência industriais é caracterizado por uma variedade de cargas não lineares, como fornos elétricos a arco, acionamentos elétricos, etc. Além disso, a elevada penetração de fontes renováveis de energia e a presença de redes com baixo nível de curto-circuito têm motivado estudos relacionados ao compensador síncrono estático (STATCOM, do inglês *static synchronous compensator*) com capacidade de injeção de corrente de sequência positiva e negativa. Nesse contexto, uma atenção especial é dada à solução baseada em conversor modular multinível (MMC, do inglês *modular multilevel converters*) devido à alta escalabilidade, modularidade, redundância e eficiência, que são características inerentes à topologia. Para ser capaz de atuar em altos níveis de tensão, é necessário associar um grande número de dispositivos eletrônicos de potência, o que pode afetar a confiabilidade do conversor. Dessa forma, métodos de tolerância a falhas podem ser empregados ao conversor, visando alcançar os requisitos de confiabilidade. No entanto, o projeto adequado do MMC para atingir uma determinada meta de vida útil ainda é uma área importante a ser explorada. Este trabalho propõe um projeto orientado à confiabilidade baseado em métodos de tolerância a falhas. A metodologia proposta permite ao engenheiro de projeto selecionar a solução de MMC mais adequada de acordo com o *trade-off* entre o custo do conversor e o requisito de confiabilidade. Além disso, o MMC baseado em observador de modo deslizante é empregado com o objetivo de aliviar o sistema de aquisição de dados, uma vez que são desprezadas as medições de tensão dos capacitores. O estudo de caso é baseado em um MMC-STATCOM de 13,8 kV/17 MVA. A implementação do conversor é baseada em quatro tensões de bloqueio comerciais de dispositivos semicondutores (1,7, 3,3, 4,5 e 6,5 kV) e quatro métodos de tolerância a falhas. Resultados experimentais são obtidos em um protótipo MMC de escala reduzida para validar a proposta. Os custos de capital (CAPEX, do inglês *capital expenditure*) e os custos operacionais (OPEX, do inglês *operational expenditure*) são estimados considerando os critérios de confiabilidade exigidos. Considerando como objetivo 10 anos de operação para o conversor e níveis de confiabilidade maiores que 90%, os projetos baseados em dispositivos de 1,7 kV com redundância em espera apresentam o menor custo para a realização do MMC-STATCOM.

Palavras-chave: conversor modular multinível; STATCOM; confiabilidade; observador de modo deslizante; métodos de tolerância a falhas; custos do conversor modular multinível.

Abstract

The current industrial electrical power systems scenario is characterized by a variety of nonlinear loads such as electric arc furnaces, electric drives, etc. Additionally, weak power systems and the high penetration of renewable power plants have motivated studies about static synchronous compensator (STATCOM) with positive and negative sequence current injection capability. In this context, particular attention is given to the solution based on modular multilevel converter (MMC) due to the high scalability, modularity, redundancy and efficiency that are inherent features of the topology. In order to operate at high voltage levels, a higher number of power electronic components is required, compromising the converter reliability. Under such conditions, fault-tolerance methods can be employed to fulfill the converter reliability requirements. However, the correct MMC design to reach a desired lifetime target is still an important area to be explored. Therefore, this work proposes a reliability-oriented design based on fault-tolerance methods. The proposed methodology allows the design engineer to select the most suitable MMC solution according to the trade-off between the converter cost and the reliability requirement. Moreover, the MMC based on sliding-mode observer is employed aiming to reduce the burden of the data acquisition system. The case study is based on a 13.8 kV/17 MVA MMC-based STATCOM. The implementation of the converter is performed through four commercial blocking voltage of semiconductor devices (1.7, 3.3, 4.5 and 6.5 kV) and four different fault-tolerant methods. Experimental results are obtained in a downscaled MMC prototype to validate the proposal. The capital expenditure (CAPEX) and operational expenditure (OPEX) are estimated considering the required reliability criteria. Considering a target of 10 years of operation for the converter and reliability levels greater than 90%, the design based on 1.7 kV devices with standby redundancy have the best cost-benefit for the MMC-based STATCOM.

Keywords: modular multilevel converter; STATCOM; reliability; sliding-mode observer; fault-tolerance methods; MMC costs.

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List of abbreviations and acronyms

ABB	Asea Brown Boveri (Swedish-Swiss multinational corporation)
ADALINE	Adaptive Linear Neuron
ac	Alternating Current
ALR	Active Redundancy with Load-Sharing
APS	Auxiliary Power Supply
AR	Active Redundancy without Load-Sharing
CAPEX	Capital Expenditure
CAU	Christian-Albrechts-Universität zu Kiel
CHB	Cascaded H-bridge
CM	Controlled Mode
CPE	Chair of Power Electronics
CVI	Capacitor Voltage Increasing
dc	Direct current
DfR	Design for Reliability
DFT	Discrete Fourier Transform
DSOGI-PNSE	Double Second-Order Generalized Integrator
EMI	Electromagnetic interference
FACTS	Flexible ac transmission systems
FB	Full-bridge
FB-MMC	Full-bridge Modular Multilevel converter
FC	Flying Capacitor
FFT	Fast Fourier Transform
FIT	Failure in time

FZSV	Fundamental Zero-Sequence Voltage
GaN	Gallium Nitride
GE	General Electric
GESEP	Power Electronics and Power Systems UFV laboratory (Gerência de Especialistas em Sistemas Elétricos de Potência)
GDU	Gate-Drive Units
GTO	Gate Turn-Off Thyristors
HB	Half-bridge
HB-MMC	Half-bridge Modular Multilevel converter
HV	High Voltage
HVDC	High-Voltage Direct Current
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristors
LV	Low Voltage
LVRT	Low-Voltage Ride-Through
MAF	Moving Average Filter
MMC	Modular Multilevel Converter
MSC	Mechanically Switched Capacitor
MSI	Mixed Sequence Injection
MSR	Mechanically Switched Reactor
MV	Medium Voltage
NPC	Neutral Point Clamped
NPV	Net Present Value
NS	Natural Rectifying Mode
NS	Neutral Shift

NSI	Negative Sequence Injection
OCFM	Open-Circuit Failure Mode
OPEX	Operational Expenditure
PCB	Printed Circuit Board
PIM	Plastic IGBT Module
PLECS	Piecewise Linear Electrical Circuit Simulation
PoF	Physics-of-Failure
PPI	Press-Pack IGBT
PR	Proportional Resonant
PSC-PWM	Phase-Shifted Carrier Pulse Width Modulation
PSI	Positive Sequence Injection
pu	Per unit
PWM	Pulse-Width Modulation
RBD	Reliability Block Diagram
RLS	Recursive Least Square
rms	Root Mean Square
RXPE	Rongxin Power Electronic Co. Ltd.
SC	Synchronous Condensers
SCFM	Short-Circuit Failure Mode
SiC	Silicon Carbide
SM	Submodule
SR	Standby Redundancy
SSSC	Static Synchronous Series Compensator
STATCOM	Static Synchronous Compensator
SVC	Static var Compensator
SVM	Space-Vector Modulation

TCR	Thyristor Controlled Reactors
TCSC	Thyristor controlled Series Capacitor
TSC	Thyristor Switched Capacitors
TSR	Thyristor Switched Reactors
THD	Total Harmonic Distortion
THVI	Third Harmonic Voltage Injection
var	Reactive Power
VSC	Voltage Source Converter
Y-CHB	Star-connected Cascaded H-bridge
ZSVI	Zero-Sequence Voltage Injection
Δ-CHB	Delta-connected Cascaded H-bridge

List of symbols

A_h	Heatsink surface area
A_p	Total area product of the cores of the converter inductors
$B_y(t)$	Operation time at which y percent of devices fail
C	SM capacitance
C_{nom}	Nominal SM capacitance
C_{h-f}	Heatsink-to-fluid thermal capacitance
C_{17},C_{33},C_{45},C_{65}	Case studies for MMC-based STATCOM
c_h	Specific heat capacity
D_1	Bottom anti-parallel diode of the half-bridge SM
D_2	Top anti-parallel diode of the half-bridge SM
d_h	Heatsink thickness
E_c	Converter energy consumption
E_{cap}	Energy stored in SM capacitors
f_c	SM carrier frequency
f_{ef}	Effective converter output frequency
f_{fc}	Fluid flow convection coefficient
f_g	Grid frequency
f_s	Sampling frequency
f_{ma}	Moving average filter frequency
f_{us}	Device utilization factor
g_n	Duty cycle of the nth SM upper-switch (S_2)
I_{max}	Converter current limit
I_{svc}	Rated device current

i_{avg}	Average current of the converter arm
i_{arm}	Arm current on the generic MMC arm
$i_{arm,l}$	Lower arm current
$i_{arm,u}$	Upper arm current
i_c	Converter circulating current
i_c^*	Converter circulating current reference
i_{D1}	Currents flowing through the semiconductor device D_1
i_{D2}	Currents flowing through the semiconductor device D_2
i_g	Grid current
$i_{g,\alpha\beta}$	Grid current in stationary reference frame
$i_{g,dq}$	Grid current in synchronous reference frame
i_{S1}	Currents flowing through the semiconductor device S_1
i_{S2}	Currents flowing through the semiconductor device S_2
K_{a1}	Circuit breaker 1
K_{a2}	Circuit breaker 2
K_c	Price per switching power
K_{cap}	Cost of the SM capacitors
K_{mag}	Cost of the magnetic devices
K_o	Price per kilowatt-hour
K_{sw}	Cost of power electronics
$k_{p,b}$	Proportional gain for individual balancing control
L_{arm}	Arm inductance
L_g	Equivalent grid inductance
m	Modulation index
$m_{arm,u}$	Ideal modulation signal of upper arm
m_{max}	Maximum modulation index

N	Number of non-redundant SMs per arm
$N_d(t)$	Number of surviving devices at time t
N_f	Number of SM failures
N_{mag}	Number of the converter inductors
N_o	Number of operating SMs
N_R	Number of redundant SMs per arm
N_s	Number of SMs per set
$N_{signals}$	Number of measured signals
N_T	Total number of SMs per arm
P	Instantaneous active power
P^*	Instantaneous active power reference
$P_{A_j}(t)$	Probability of the MMC arm in state j considering the ALR method
$P_{C_j}(t)$	Probability of the MMC arm in state j considering the CVI method
$P_{S_j}(t)$	Probability of the MMC arm in state j considering the SR method
P_{12}	Active power flow from bus 1 to bus 2
p_{sm}	Instantaneous SM power of a generic MMC arm
Q	Instantaneous reactive power
Q^*	Instantaneous reactive power reference
Q_f	Finite index set
Q_{12}	Reactive power flow from bus 1 to bus 2
q_n	Gate signals applied to the nth SM upper-switch (S_2)
R_{ac}	Ac-side charging resistance
R_{arm}	Arm inductor resistance
R_b	Bleeder resistor
R_g	Equivalent grid resistance
R_{h-f}	Heatsink-to-fluid thermal resistance

$R(t)$	Reliability function
S_n	Converter nominal power
S_T	Bypass structure
S_1	Bottom IGBT of the half-bridge SM
S_2	Top IGBT of the half-bridge SM
T_a	Ambient temperature
T_c	Switching period
T_j	Junction temperature
V_1	Voltage magnitude in the bus 1
V_2	Voltage magnitude in the bus 2
V_g	Line-to-line converter output voltage rms value
V_{lf}	Lyapunov function candidate
V_s	Line-to-line converter output voltage rms value
V_{sn}	Line-to-neutral converter output voltage rms value
V_{svc}	Semiconductor blocking voltage capability
V_{th}	Hysteresis band voltage
v_{ac}	Instantaneous ac grid voltage
v_{an}	Line-to-neutral voltage of the phase A
v_{arm}	Voltage on the generic MMC arm
$v_{arm,l}$	Voltage on the lower MMC arm
$v_{arm,u}$	Voltage on the upper MMC arm
v_{avg}	Average voltage of all SM capacitors
v^*_{avg}	Reference value for average capacitor voltages
v_b	individual balancing voltage
v_c	Converter internal voltage
$v_{f,n}$	SM capacitor voltage filtered

$v_{l,n}$	Normalized reference signals per phase of the lower arm
v_n	SM capacitor voltage
$v_{u,n}$	Normalized reference signals per phase of the upper arm
v_{dc}	Converter dc-link voltage
v_g	Grid effective line-to-neutral voltage
$v_{g,\alpha\beta}$	Grid voltage in stationary reference frame
$v_{g,dq}$	Grid voltage in synchronous reference frame
v_r	Ratio of the applied voltage to the nominal voltage
v_s	Effective line-to-neutral voltage synthesized by the converter
$v_3 s$	1/6 of third harmonic of the phase voltage
T_{ma}	Window time of the moving-average filter
t	Operation time
t_0	Target operation time
x_{eq}	Converter output reactance
Z_{c-h}	Case-to-heatsink thermal impedance
Z_{h-f}	Heatsink-to-fluid thermal impedance
Z_{j-c}	Junction-to-case thermal impedance
Z_T	Transmission line impedance
α_d	Decrease factor
α_r	Maximum current rise rate
β_c	Angular displacement between the carrier waveforms in the upper and lower arms
δ	Per unit SM voltage ripple
δ^+	Positive sequence voltage angle
δ^-	Negative sequence voltage angle
δ_1	Voltage phase angle of the bus 1

δ_2	Voltage phase angle of the bus 2
δ_m	Modulation margin in practical application
Δi_c	Peak-to-peak circulating current ripple
ΔV	SM capacitor voltage ripple from average to peak (or valley)
ΔV_{dc}	Dc-link voltage ripple
ΔV_g	Maximum variation assumed in the grid voltage
ΔQ	Reactive power errors
Δx_{eq}	Maximum variation assumed in the output reactance
ϵ	Worst-case discrepancy in SM capacitance
η	Voltage stress factors
κ_h	Thermal conductivity of the heatsink material
λ	Observer correction gain
λ_b	Component base failure rate
λ_{SM,A_j}	failure rate of an SM upon j SMs failure considering the ALR method
λ_{SM,C_j}	failure rate of an SM upon j SMs failure considering the CVI method
λ_{SM,S_j}	failure rate of an SM upon j SMs failure considering the SR method
$\lambda(t)$	Failure rate
ϕ	Phase difference between grid voltage and current
φ	Perturbation term
ρ_h	Material density of the heatsink
τ	RC time constant to discharge the SM capacitor
$\theta_{l,n}$	Angular displacements of the lower carrier waveforms
$\theta_{u,n}$	Angular displacements of the upper carrier waveforms
θ_z	Angle that define the zero crossing of the current arm
ω_g	Angular grid frequency

Superscripts

$*$	Reference value
s	Instantaneous (switched) value
$+$	Positive sequence system
$-$	Negative sequence system

Subscripts

arm	Generic MMC arm
f	Related to SM failures
l	Generic MMC lower arm
MMC	Generic converter
SM	Generic SM at the generic MMC arm
u	Generic MMC upper arm
$\alpha\beta$	Variable in stationary reference frame

Contents

1 Introduction

1.1 Context and Relevance

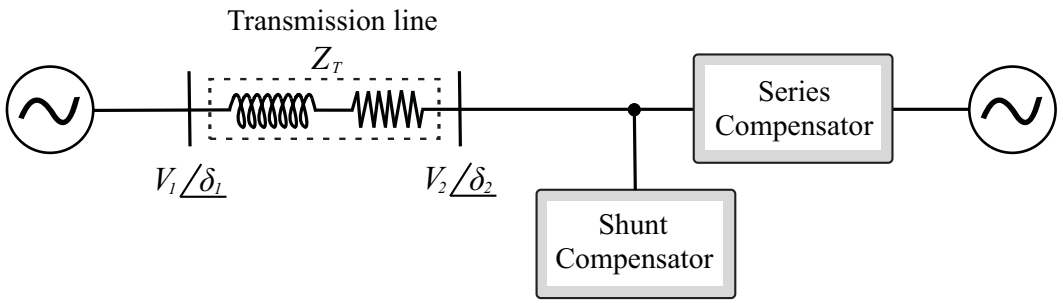
The current power systems scenario is composed of complex structures requiring careful operation, design and planning. The presence of non-linear loads (such as electric arc furnaces, high-power full controlled devices, etc.) and high penetration of solar and wind power plants result in power quality deterioration and grid voltage fluctuations (Ma; Huang; Zhou, 2015; Blaabjerg et al., 2006).

Improving power system flexibility is essential to ensure uninterrupted services while managing changes in supply and demand. Under such conditions, the Flexible AC Transmission Systems (FACTS) have been developed to improve the performance of weak alternating current (ac) power systems and to enhance transmission capabilities over long ac lines (Hingorani; Gyugyi, 1999).

Some FACTS devices are used to compensate the reactive power (var) in ac power systems, which is indicated to improve the performance at the transmission and distribution levels (Benidris et al., 2016). The reactive power compensators can be classified into series or shunt compensators, as shown in Fig. 1, where V_1, V_2, δ_1 and δ_2 are the voltage magnitude and the voltage phase angle at the first and the second bus, respectively. Moreover, Z_T is the line impedance. Therefore, the two categories of var compensators have the following function:

- Series compensators: these devices inject voltage in series with the line, modifying the transmission or distribution line impedance Z_T.
- Shunt compensators: these devices inject current into the power system, controlling the voltage V_2 at a given bus.

Figure 1 – Schematic of FACTS controllers for reactive power compensation with series compensation or shunt compensation.



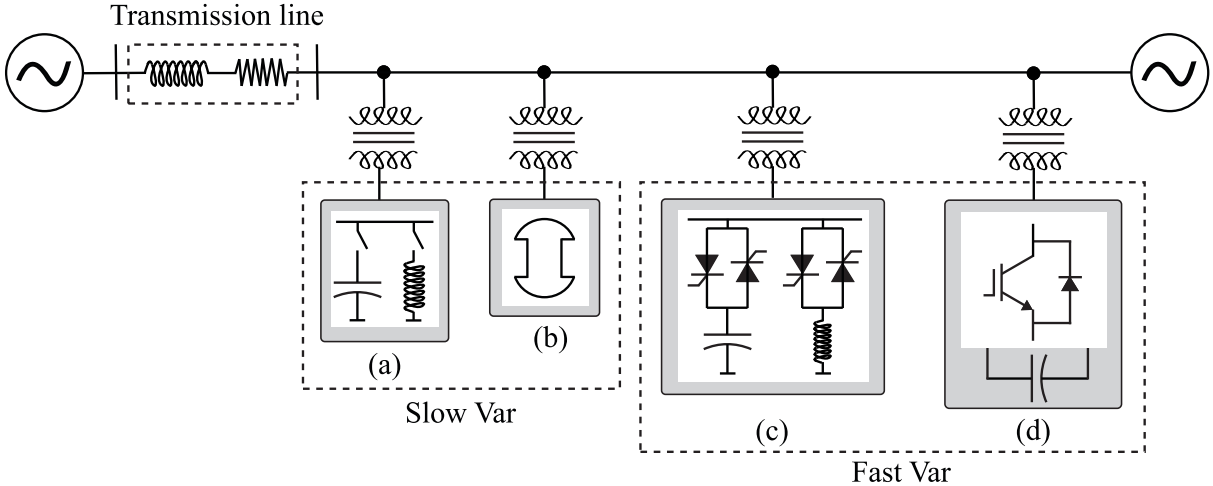
Source: Elaborated by the author.

Thyristor controlled series capacitor (TCSC) and static synchronous series compensator (SSSC) are examples of devices used for series compensation. The compensated reactive power is a function of the current flowing through the TCSC, which is a drawback of this approach. Moreover, an inherent problem of series compensators arises during faults, since the structure must be designed to support the fault currents if the var compensation is required under such conditions. Otherwise, a bypass structure must be employed. Therefore, shunt compensators offer certain advantages over series compensators, even though their primary limitation lies in their ability to provide dynamic control of power flow and system stability.

Due to simplicity and low cost, mechanically switched capacitor (MSC) and mechanically switched reactor (MSR) banks are widely used as shunt compensators, as illustrated in Fig. 2 (a). However, these topologies are not fully controlled, limiting their use to situations where the reactive power compensation range is low (Dixon et al., 2005). Figure 2 (b) shows the Synchronous Condenser (SC). A synchronous machine is connected to the power system which can exchange reactive power. However synchronous condensers require substantial foundations and a significant amount of starting and protective equipment (Igbinovia et al., 2015). Besides, they contribute to the short-circuit current, have slow response in case of rapid load changes, higher losses and operating costs than other technologies for reactive power compensation.

The Static var Compensator (SVC), as shown in Figure 2 (c), can compensate lead and lag reactive power variably by controlling the thyristor switching angle aiming to solve this issue. The SVC may consist of one or more of the following active elements (Manfredo Lima; Stig L. Nilsson, 2020):

Figure 2 – Shunt compensators: (a) Mechanically Switched Capacitor/Reactor; (b) Synchronous Condensers (SC); (c) Static var Compensator (SVC); (d) Static Synchronous Compensator (STATCOM).



Source: Elaborated by the author.

- Thyristor Controlled Reactors (TCR), which provide continuously varying inductive reactive power according to the firing angle of the thyristors.
- Thyristor Switched Capacitors (TSC), which provide capacitive reactive power changed in discrete mode (ON/OFF), when thyristor valves are fully conducting or totally blocking the current flow.
- Thyristor Switched Reactors (TSR), which provide inductive reactive power changed in discrete mode (ON/OFF), when thyristor valves are fully conducting or totally blocking the current flow.

Nevertheless, the SVC injects low-order harmonic currents into the grid, which requires a large amount of passive filters (Igbinovia et al., 2015). In addition, the SVC reactive power output is proportional to the square of the voltage magnitude. In other words, SVCs give less support to the grid at the time of greatest need such as in applications to prevent system voltage collapse and motor stalling conditions (Colin Davidson; Marcio M. de Oliveira, 2020).

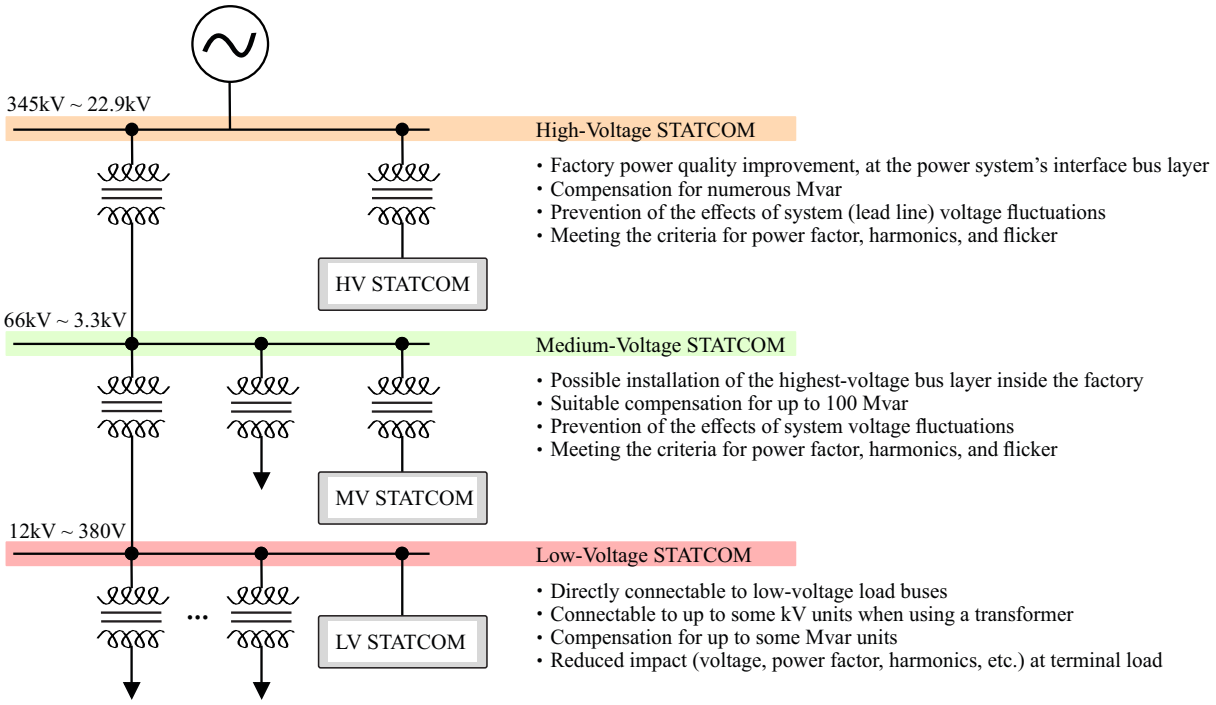
The Static Synchronous Compensator (STATCOM) is a highly recommended technology for reactive power compensation in electrical power networks (Shahnia; Rajakaruna; Ghosh, 2014; Igbinovia et al., 2015; Ma; Huang; Zhou, 2015). As illustrated in Fig. 2 (d), this technology consists of a Voltage Source Converter (VSC) that exchanges reactive power with the grid. In comparison to SVC, STATCOM presents higher power density, higher efficiency and no contribution to short-circuit currents (Chakraborty et al., 2012). In addition, a fast dynamic response is achieved because mechanical inertia as in traditional synchronous compensators is avoided. These features make the STATCOM suitable for reactive support during fast transients.

The main drawback of STATCOM is the higher cost, when compared to SVC systems. Nevertheless, the technical benefits and recent advances in power converters technology have led to the use of VSC topologies instead of thyristor based systems (Behrouzian, 2016). Table 1 summarizes the main features observed in the FACTS controllers (Kadandani; Maiwada, 2015).

Table 1 – Comparison among FACTS controllers.

Device	Dynamic of response	Power quality	Steps	Inertia	Cost
MSC/MSR	Slow	Low	Fixed	No	Low
TSC	Fast	Low	Fixed	No	Medium
TCR	Fast	Low	Continuous	No	Medium
SVC	Fast	Low	Continuous	No	Cheaper than STATCOM
SC	Slow	High	Continuous	Yes	High
STATCOM	Fast	High	Continuous	Possible	High

Figure 3 – FACTS solution according to the applied system characteristics.



Source: Adapted from LSElectric (2020).

Different power and voltage levels can be employed in STATCOM applications, as illustrated in Fig. 3. As observed, the STATCOM can be connected to systems with hundreds of kV. Therefore, challenges arise about the design of the STATCOM converter due to the limitation of the blocking voltage of commercial semiconductor devices. For this reason, different multilevel converters have been investigated as possible candidates for STATCOM realization over the years. The next section discusses the main STATCOM architectures employed in medium- and high-voltage applications.

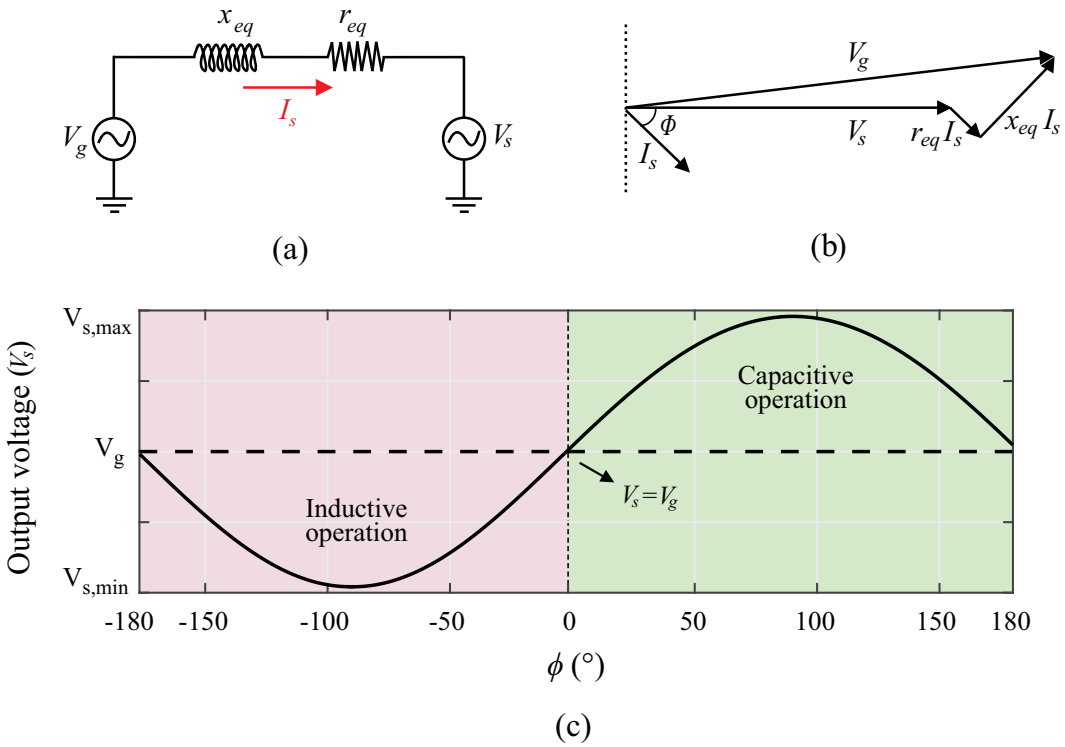
1.2 STATCOM Operating Principle and Realization

This section describes the STATCOM operating principle and the development of conventional STATCOM realizations and the promising STATCOM realizations based on cascaded multilevel converters.

1.2.1 STATCOM Fundamentals

The operating principle of the STATCOM can be explored using a simplified model (Mendonça et al., 2022), depicted in Fig. 4 (a). In this model, the exchange of reactive power between the STATCOM and the grid is controlled by adjusting the magnitude of the converter synthesized rms voltage (V_s), either higher or lower than the rms grid voltage (V_g). This voltage adjustment is highlighted in the phasor diagram shown in Fig. 4 (b).

Figure 4 – STATCOM average model; (b) Phasor diagram of STATCOM. (c) Output voltage (rms) synthesized by the converter.



Source: Adapted from Mendonça et al. (2022).

Furthermore, the impact of varying the operating angle (ϕ) is demonstrated in Fig. 4 (c). It is important to remark that the STATCOM operation mode is adopted in accordance to the definition described in Akagi, Watanabe and Aredes (2007). As noted, there are three distinct operating conditions:

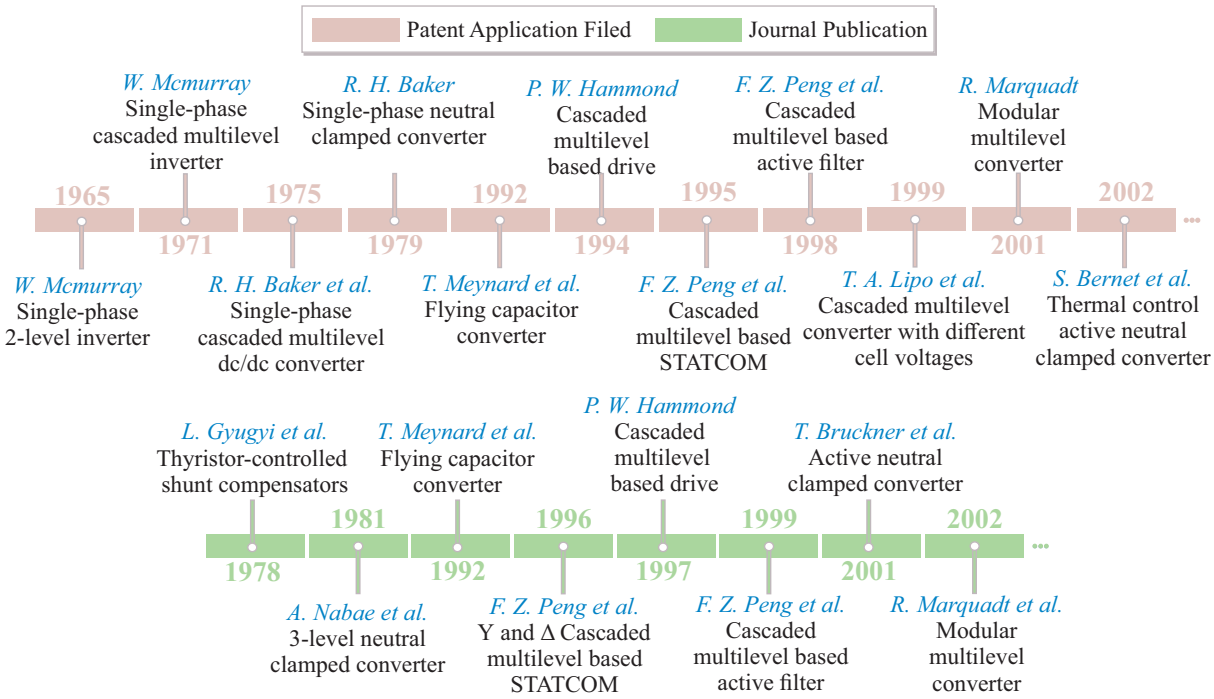
- $V_g < V_s$, STATCOM performs a capacitive operation;
- $V_g > V_s$, STATCOM performs an inductive operation;
- $V_g = V_s$, there is no reactive power exchange between the STATCOM and the grid;

1.2.2 Conventional STATCOM Realization

The major challenge in STATCOM realization is to design a converter topology which must reach high power and voltage levels with standard rated semiconductor switches (Fujii; Schwarzer; De Doncker, 2005; Muñoz et al., 2014). In this sense, the main scientific contributions (measured in terms of patents and journal papers) to the development of power converters employed in the STATCOM market are illustrated in Figure 5.

The traditional realizations of a high-power converter with low-harmonic content have involved two-level VSC, neutral point clamped (NPC) and flying capacitor (FC)

Figure 5 – Timeline of the main contributions in the development power converters employed in the STATCOM market.



Source: Adapted from Cupertino (2019).

topologies. Even though NPC is considered multilevel topologies, the number of levels is usually limited to five or seven in practical applications (Fujii; Schwarzer; De Doncker, 2005). Using transformers to decrease voltage levels is feasible, although it has the disadvantages of being bulky and heavy. Additionally, the efficiency of the converter may be compromised, particularly at high power and lower voltages levels, due to the higher current requirements. Under such conditions, the high kV units necessary to connect the STATCOM to the grid must be reached by series-connected semiconductor devices, since the maximum blocking voltage of the semiconductors commercially available is limited. The advances in silicon carbide (SiC) and gallium nitride (GaN) devices can bring an increase of some kV units to the typical high-power silicon IGBT modules that reaches 6.5 kV. However, some practical issues of the series-connected solution will still be present, such as voltage equalization between the series switches and fault-tolerant operation (Shammas; Withanage; Chamund, 2006).

Another solution is combining several conventional two-level VSC with complex magnetic circuits (Colin Davidson; Marcio M. de Oliveira, 2020). These magnetic circuits make the STATCOM bulky and heavy, and affects the overall efficiency (Hagiwara; Akagi, 2009). According to Peng et al. (1996), field experiences show the transformer can produce about 50% of the total losses, occuping up to 40% of the system space and hamper the control due to inrush currents and saturation effects.

Table 2 presents some STATCOM currently available in the market based on the

Table 2 – VSC topologies for STATCOM applications.

Converter Configuration	Trade Mark	Manufacturer	Grid voltage
Two-level VSC + Transformer	VArPro^{TM}	Hitachi-ABB	480 V to HV[1]
	PCS 100	Hitachi-ABB	480 V
	SVG Statcom	Severn	6 kV to 55 kV
Three-level VSC (NPC) + Transformer	PCS 6000	Hitachi-ABB	10 kV to HV[1]
	GRIDCON®	MR	3 kV to 35 kV
	SMART Q^{TM}	HYOSUNG	HV[1]

[1]High Voltage. The maximum voltage value is not specified.

aforementioned solutions. It is important to note that the converter voltage is increased through a step-up transformer before connecting to the grid. Consequently, the current will be high in the low voltage side which leads to higher power losses. This fact led the research community to focus on transformerless solutions, to directly connect the converter into the grid (Behrouzian; Bongiorno; De La Parra, 2013).

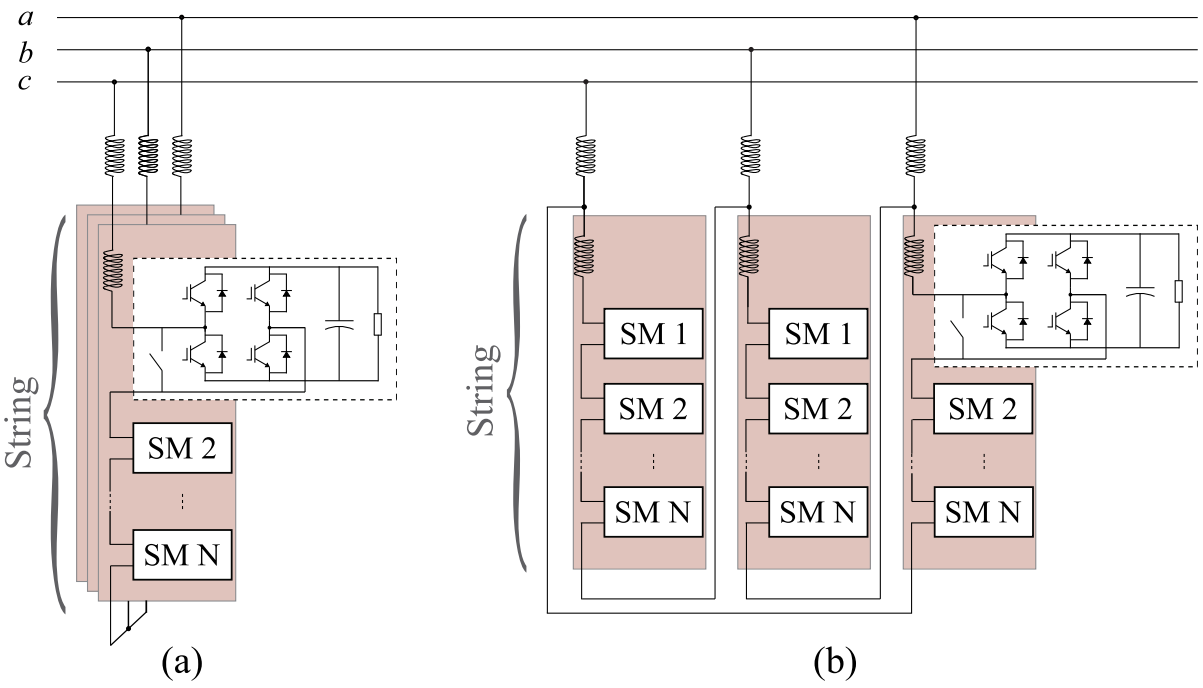
1.2.3 Cascaded Multilevel Converters

A widely used alternative for medium/high-voltage systems is the cascaded multilevel converters (Mcmurray, 1971; Marquardt, 2001; Lesnicar; Marquardt, 2003), which are based on series connection of submodules (SMs). These SMs, also called cells, employ medium-voltage devices to obtain a converter with higher voltage capability. The following advantages of cascaded multilevel topologies can be highlighted (Franquelo et al., 2008):

- Low switching frequency can be employed, which results in high efficiency;
- A high number of levels can be reached, resulting in low harmonic contents in the output voltage and current;
- Low voltage steps (dv/dt), which reduce stresses in the insulation of any equipment connected at the converter output;

The cascaded connection of full-bridge SMs date back to the 1970s for single-phase systems (Mcmurray, 1971; Baker; Bannister, 1975). The three-phase STATCOM based on both Y- and Δ-connected cascaded H-bridge converter (CHB) were proposed in 1996 by Peng et al. (1996). The three-phase Y- and Δ-connected CHB topologies are illustrated in Fig. 6 (a)-(b). The CHB was first adopted by Alstom for high-power STATCOM employing gate turn-off (GTO) thyristors in the full bridge SMs (Ainsworth et al., 1998). Nowadays, this concept is widespread in the industry and most products are based on IGBTs (Insulated Gate Bipolar Transistors) or press-pack IGCTs (Integrated Gate-Commutated Thyristors) (Sharifabadi et al., 2016).

Figure 6 – Schematic of the three-phase CHB: (a) star-connected; (b) delta-connected.



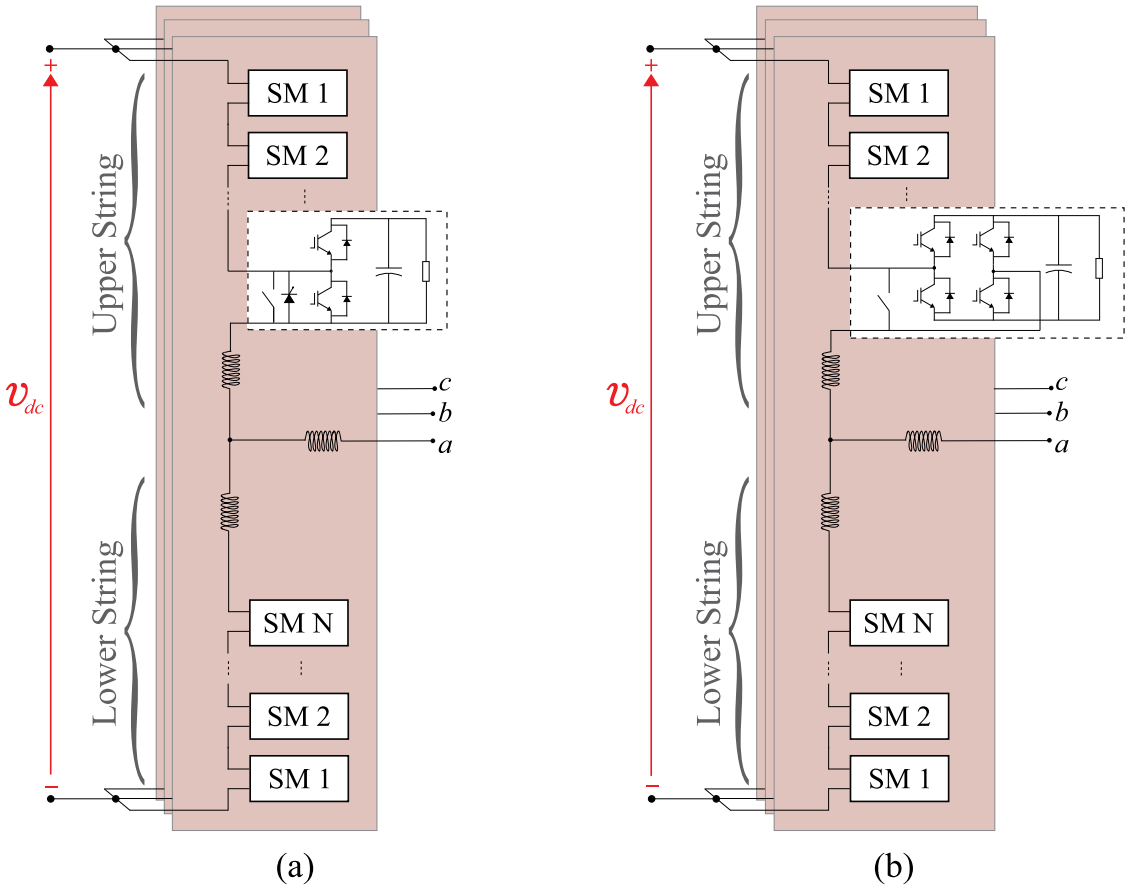
Source: Elaborated by the author.

The modular multilevel converter (MMC) was originally proposed in 2001 in a German patent by Prof. Marquardt (Marquardt, 2001). The direct current (dc) to three-phase converter structure with series-connected SMs is illustrated in Fig. 7. The use of half-bridge SMs, as well as full-bridge SMs, is allowed due the presence of two strings, also called arms, for each phase of the MMC. Another notable feature observed in the MMC is the presence of a commmon dc-link, as observed in traditional two-level converters (Lesnicar; Marquardt, 2003). These features have made the MMC attractive and commercially successful mainly for high-voltage direct current (HVDC) systems. It is important to remark that the HVDC schemes are often operated in "STATCOM mode" when the real power is zero, being possible to implement a purpose-built STATCOM from this topology (Colin Davidson; Marcio M. de Oliveira, 2020).

As observed, MMC and CHB use the same concept of series connection of SMs. However, the original MMC topology presents two string per phase (upper string and lower string). Therefore, to avoid confusion regarding the terminology of these topologies, the following classification will be utilized in this work:

- Star-connected Cascaded H-bridge (Y-CHB), as presented in Fig. 6 (a);
- Delta-connected Cascaded H-bridge (Δ-CHB), as presented in Fig. 6 (b);
- Half-bridge Modular Multilevel converter (HB-MMC), as presented in Fig. 7 (a);
- Full-bridge Modular Multilevel converter (FB-MMC), as presented in Fig. 7 (b).

Figure 7 – Schematic of the three-phase MMC: (a) half-bridge SM; (b) full-bridge SMs.



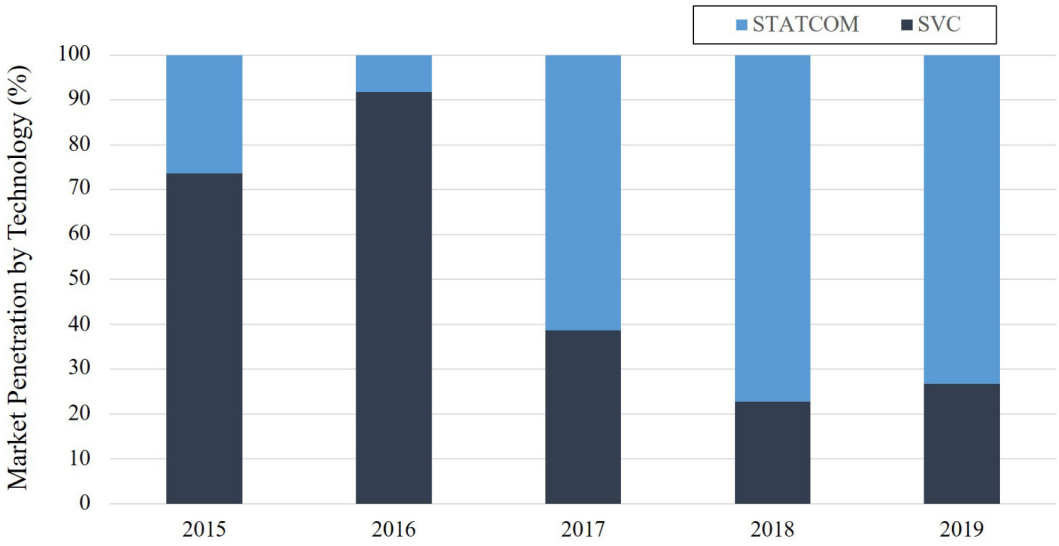
Source: Elaborated by the author.

1.3 Trends for STATCOM

Due to the geographical arrangement of renewable energy generation, the distance to the consumption centers is growing in many countries. In Germany, for instance, large wind farms feed into the grid in the north while the load centers are located in other parts of the country. For a long time, large power plants have provided the reactive power necessary for the grid stabilization. However, many of these conventional power plants are being taken off the grid due to the energy transition, requiring the use of FACTS. SVC technology dominated the FACTS market for decades. However, the penetration of STATCOM in the market has grown over the last few years, as observed in Fig. 8. In this refereed period, the main player in the market is Siemens, followed by Hyosung, RXPE, NR Electric and Hitachi-ABB (Baig, 2021).

The latest efforts of manufacturers and researchers have focused on cascaded multilevel converters based STATCOM for medium- and high-voltage systems. Currently, research on STATCOM is motivated by some factors such as cost reduction, reliability, modern grid codes requirements and hybrid solutions.

Figure 8 – Market penetration by the main FACTS technologies in the last years.



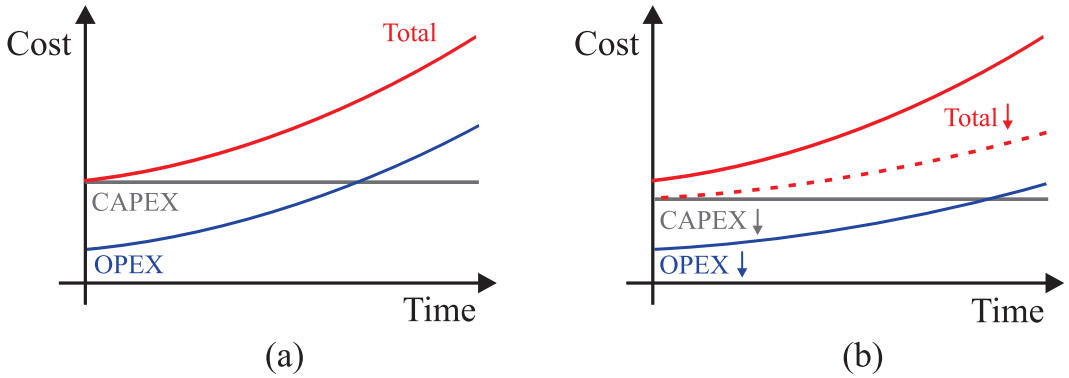
Source: Adapted from Baig (2021).

1.3.1 Overall Cost Reduction and Reliability Improvement

The overall product cost is generally related to the capital expenditure (CAPEX) and operational expenditure (OPEX), as observed in Fig. 9 (a). Regarding STATCOM applications, CAPEX is mainly related to the converter cost: capacitors, magnetic devices, semiconductor devices, controllers, PCBs, cooling system, and others. Efforts are made to ensure CAPEX reduction in the initial phase of the converter design, as shown in Fig. 9 (b). In this context, some approaches aim to reduce the number of components, such as capacitors, sensors, semiconductor devices and their drive circuits (Prabaharan; Palanisamy, 2017; da Silva; Vieira; Rech, 2018; Saif et al., 2018).

Since STATCOM are hot-standby devices, the converter efficiency and

Figure 9 – Converter cost related to CAPEX and OPEX: (a) Conventional approach; (b) Reduction trend in STATCOM costs.



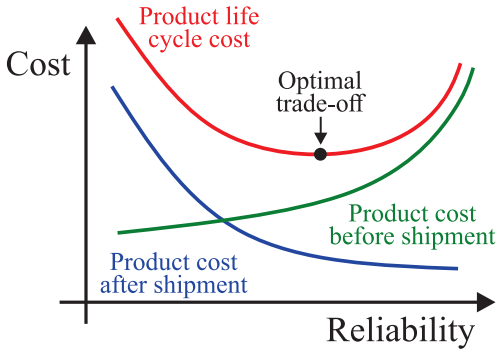
Source: Elaborated by the author.

non-scheduled maintenance are factors which affects the benefit-cost ratio of the modern STATCOM (Tu; Yang; Wang, 2019). The net present value (NPV) of the power losses over the STATCOM lifetime (around 20 years), brought forward to the time of purchasing the STATCOM, can be comparable to the CAPEX (Colin Davidson; Marcio M. de Oliveira, 2020), as shown in Fig. 9 (a). In addition, Figure 10 describes a general optimization curve to define the reliability specification of a product in terms of achieving minimum life cycle cost (Wang; Liserre; Blaabjerg, 2013). The product cost before shipment is mainly related to the manufacturing cost such as design, development and production phases. Therefore, the cost of correcting the deficiencies in the design phase is increased according to the product development proceeds. On the other hand, a low failure rate during field operations results in low maintenance costs, as shown in product cost after shipment curve. These factors drive research that seek to increase the reliability and efficiency of the STATCOM (Zheng et al., 2019; Koyama et al., 2018), which leads to a reduction in the OPEX indicated in Fig. 9 (b).

To reduce the failure rate during field operations of power converters, the most fragile components must be identified. (Yang et al., 2011) conducted a survey with semiconductor manufacturers, integrators, and users in the aerospace, automation, motor drive, utility power, and other industry sectors to address concerns related to the requirements and expectations of reliability in power electronics. As observed, Fig. 11 shows that "semiconductor power devices" and "capacitors" account for almost 50% of responses as the most fragile components. Furthermore, many industry survey participants were asked to define the elements that are most crucial to be researched to improve the reliability of power electronics converter systems (Falck et al., 2018). More than 60% of respondents expect to see more research focused on power semiconductors, power semiconductor modules and capacitors.

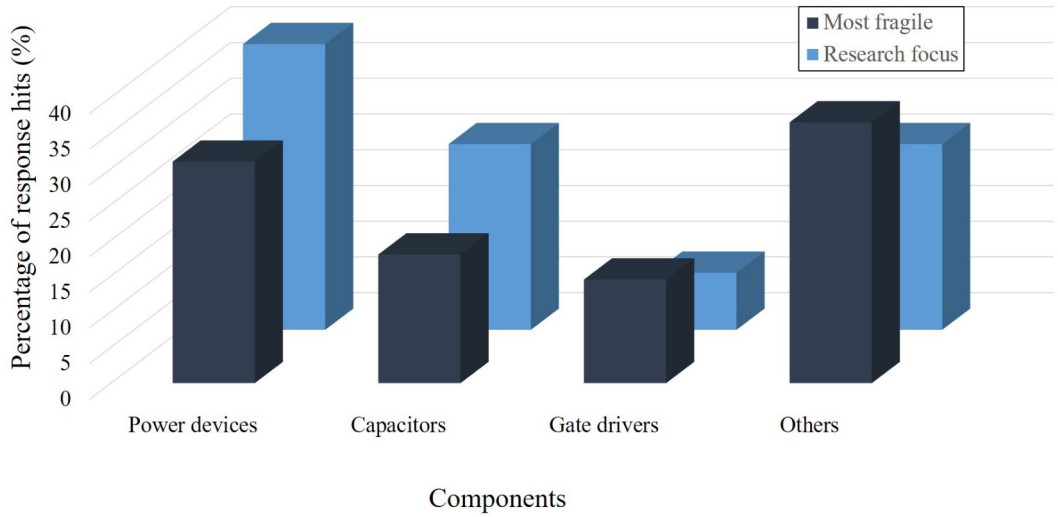
Aiming to improve the reliability of the power converter devices, the main causes of damage must be identified. In this sense, the power electronics systems are exposed

Figure 10 – The reliability impact on product cost in terms of achieving minimum life cycle cost.



Source: Adapted from Wang, Liserre and Blaabjerg (2013).

Figure 11 – Industry experts' answers to the: Black - distribution of fragile components in power converters; Blue - the components of power electronic systems that should focus on future research. *Remark:* surveys conducted in aerospace, automation, motor drive, utility power, and other industry sectors.



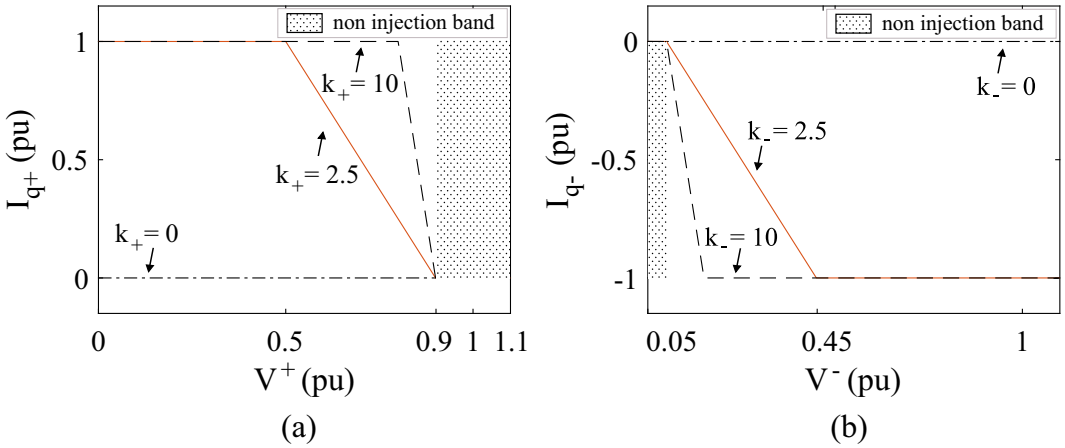
Source: Adapted from Yang et al. (2011), Falck et al. (2018).

to stressors that depend on the application and the operating conditions, such as high humidity, polution, mechanical impacts, radiation. According to Falck et al. (2018), the thermal stressors are considered particularly critical, with power cycling identified as the most consequential. In addition to these mentioned factors, concern about the reliability of current STATCOM has increased, since multilevel converters are composed of a higher number of components, which jeopardizes the converter reliability. Thus, approaches such as analytical analysis, design for reliability (DfR) and fault-tolerance schemes are solutions to evaluate and improve the reliability of power electronic converters.

1.3.2 Modern Grid Codes Requirements

The modern grid codes for renewable energy power plants requires negative sequence support during voltage sags (VDE, 2015). In Germany, for example, the technical requirements for connection to the high-voltage system includes positive and negative sequence injection during unbalanced faults, as observed in Fig. 12. Therefore, the STATCOM converter must provide negative sequence injection (Wijnhoven et al., 2014). According to Behrouzian and Bongiorno (2017), Y-CHB and Δ-CHB present a singular operation point during unbalanced conditions. If the system reaches this point, the converter will probably trip from the electrical grid and will not be able to provide voltage support (Behrouzian, 2016). Under such conditions, recent publications indicate HB-MMC and FB-MMC as the most suitable for STATCOM which are submitted to unbalanced voltage

Figure 12 – Low-voltage ride-through (LVRT) current injection in Germany: (a) Positive sequence injection requirements; (b) Negative sequence injection requirements. *Remark:* k_+ and k_- are the gain factor for the positive and negative reactive current injection, respectively.



Source: Adapted from VDE (2015).

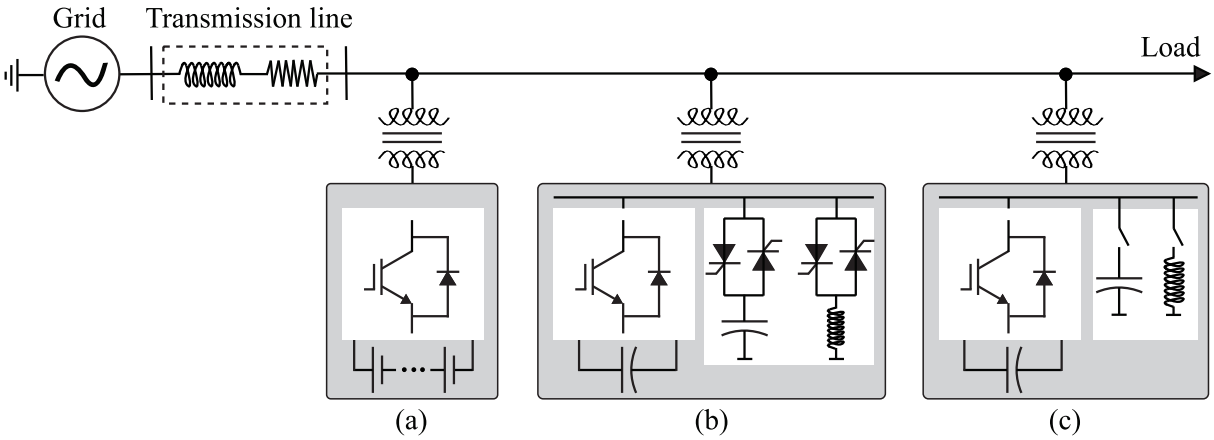
conditions (Cupertino et al., 2019a).

1.3.3 Hybrid STATCOM Solutions

STATCOM are usually custom devices that depend on the kind of application, power rated, size and weight (e.g., building, container or panel solutions). In this sense, the use of hybrid configuration is emerging, where an energy storage can be added to the conventional STATCOM to exchange active power with the grid or even another reactive power compensator can be integrated to expand the operating range. In addition, the hybrid STATCOM can offer additional benefits to those already available for traditional solutions employed for utilities.

Energy storage system integrated in STATCOM (ES-STATCOM) may be employed to provide active power support for short periods, as illustrated in Fig. 13 (a). These systems are required in future generation of power systems to provide load compensation, mitigation of voltage sags, elimination of power oscillations, frequency regulation and inertia capabilities. The distributed and centralized energy storage approaches are often employed (Wang et al., 2016). Regarding the distributed energy storage approach, low-voltage battery packs are distributed among the converter SMs. Moreover, a failure detected in one battery rack implies the absence of energy stored from only one SM. However, the integration of batteries and converter SMs under the same container leads to some thermal management issues. In the centralized energy storage approach, the storage units are concentrated in the dc-link, which allows installation in separate containers of the converter. Therefore, the ES-STATCOM can operate as a conventional STATCOM if the storage units are isolated for maintenance. Aiming to push the ES-STATCOM technology,

Figure 13 – Hybrid solution in shunt configuration: (a) ES-STATCOM; (b) STATCOM with either TSC or TSR; (c) STATCOM with either MSC or MSR.

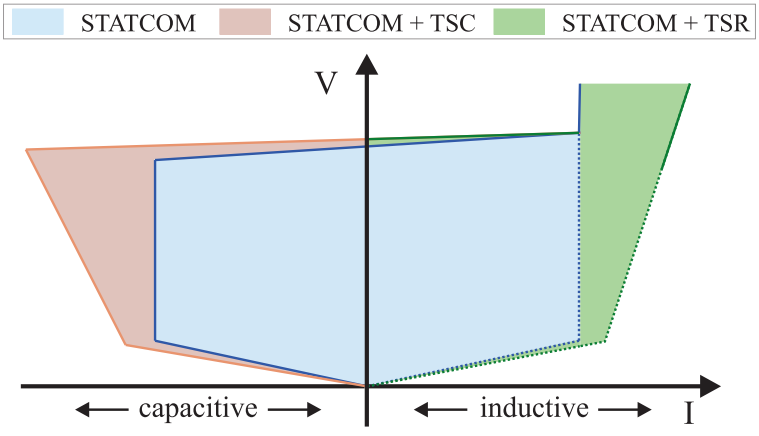


Source: Elaborated by the author.

the German-Dutch transmission system operator TenneT has awarded Siemens Energy to install the world's first STATCOM with power supply system via supercapacitors, going to operation in 2025 (SIEMENS, 2023). The available energy can be used to stabilizes grid frequency fluctuations for 1-5 seconds by charging or discharging the supercapacitors connected in the MMC dc-link.

A STATCOM has improved characteristics compared to a SVC, especially for handling undervoltages, since the STATCOM is capable of injecting full reactive power current independent from the voltage magnitude. However, conventional SVCs are better than STATCOM at suppressing temporary overvoltages due to the higher capacity of thyristors and inductors, which lead to a greater var absorption capability without any major impact on the SVC design (Colin Davidson; Marcio M. de Oliveira, 2020). Using a STATCOM to cover the whole dynamic swing range can lead to an oversizing on either capacitive or inductive Mvar output sides, as observed in Fig. 14. Therefore,

Figure 14 – VI characteristic of hybrid STATCOM with either TSC or TSR.



Source: Elaborated by the author.

combining STATCOM with either TSC or TSR technologies is an interesting approach for asymmetrical operation, as shown in Fig. 13 (b). Since no additional harmonics are generated by the thyristor branches, no ac filters are required (Siemens AG, 2016). Based on this concept, hybrid STATCOM with additional steady-state capacity can be achieved adding a mechanically switched elements (MSC or MSR) as needed, as shown in Fig. 13 (c). This kind of configuration is suitable when a dynamic reserve is desired as part of the STATCOM solution, and additional reactive capacity is needed for slow response compensation such as load flow changes, which is suppressed through MSC or MSR.

Table 3 provides a summary of some hybrid STATCOM currently available in the market by major manufacturers. It is important to remark that these solutions employ STATCOM based on Δ-CHB topology, with the exception of SVC PLUS FS, which employs MMC topology.

Table 3 – Overview of some hybrid STATCOM commercially available.

Hybrid Configuration	Manufacturer	Trade Mark	Power Range
ES-STATCOM	Siemens	SVC PLUS Frequency Stabilizer	±300 MW and ±300 Mvar
	Hitachi-ABB	DynaPeaQ 100	5 to 50 MW and ±70Mvar
STATCOM + TSC	Hitachi-ABB	Hybrid SVC Light®	-250 to +400 Mvar
	Siemens	Hybrid SVC Plus	-50 to +150 Mvar
	GE	Hybrid GE's STATCOM	-100 to +225 Mvar

1.4 Purpose and Contributions

One advantage of MMC-based topologies is the inherent fault-tolerant operation associated with the high number of SMs. Therefore, the main objective of this Ph.D thesis is to present a reliability-oriented design aiming to improve cost reduction and reliability of MMC-based STATCOM. Furthermore, the main MMC fault-tolerance methods available in the technical literature are analyzed.

Based on the general purpose, the following topics will be approached in this work:

1. *Modeling, Control and Design for MMC-based STATCOM*: this topic proposes a design of MMC-based STATCOM. Analysis of number of SMs, required SM capacitances, required current ratings of semiconductors power devices and output filter design are developed. Moreover, a dynamic response analysis of the converter is presented.

2. *Fault-tolerance schemes for MMC-based STATCOM*: this topic describes and compares critically the main MMC fault-tolerance methods available in the technical

literature. The main SMs bypass structures and the methods of fault diagnosis in MMC are presented.

3. *Reliability-Oriented Design*: a suitable MMC design that ensures a fault-tolerance operation is an important field to be explored. Therefore, this topic aims to propose a reliability-oriented design to select the most suitable MMC solution according to the trade-off between the converter cost and the reliability requirement.

The main goals related to the fault-tolerance operation are listed:

- provide an overview of the main MMC fault-tolerance schemes available in the technical literature.
- provide an overview of MMC-based STATCOM control under faulty SMs;
- analyze the limitations of each MMC fault-tolerance scheme in the occurrence of SM failures.
- proposal of a sliding-mode observer applied to MMC-based STATCOM, suitable for operation in the occurrence of SM failures.

Regarding the reliability-oriented redundancy design, the following contributions are targeted:

- evaluate the dynamic behavior, reliability level and costs of MMC-based STATCOM design. Four semiconductor blocking voltage (1.7 kV up to 6.5 kV) commercially available for Si devices are considered.
- evaluate the MMC reliability considering the critical elements such as: semiconductor power devices, capacitors, control system and bypass structure.
- evaluate the MMC reliability based on Markov Chain-based approach considering four different MMC fault-tolerance schemes.
- proposal of a *reliability vs cost* map to evaluate the trade-off of different MMC-based STATCOM solutions.

Aiming to evaluate the modeling, control and design of the converter, a case study based on a 13.8 kV/17 MVA MMC-based STATCOM is adopted. Four different fault-tolerant methods are evaluated in order to maintain the MMC operation in case of faulty SMs. The implementation of the converter is performed through four commercial blocking voltage of semiconductor devices (1.7, 3.3, 4.5 and 6.5 kV). The simulation results are obtained by PLECS environment. In addition, experimental results are obtained in

a downscaled MMC prototype to validate the control strategies and one fault-tolerance scheme. Finally, the reliability-oriented design is analytically evaluated.

The present research has been developed at Universidade Federal de Minas Gerais (UFMG) in cooperation with the Gerência de Especialistas em Sistemas Elétricos de Potência (GESEP-UFV). Experimental results has been obtained at Chair of Power Electronics (CPE) during a period working at Christian-Albrechts-Universität zu Kiel (CAU).

Furthermore, this Ph.D thesis represents a continuation of the extensive research conducted by the MMC research group of GESEP over the past 8 years, which resulted in 5 Master thesis (de Sousa, 2019; Farias, 2019; Amorim, 2019; Júnior, 2021; Mendonça, 2021) and 3 Ph.D thesis defenses (Cupertino, 2019; Pinto, 2022; de Sousa, 2022).

1.5 List of Publications

The partial results of this Ph.D project have resulted in the publication of three journal papers and one book chapter. These publications are presented as follows:

1. J. V. M. Farias, A. F. Cupertino, V. d. N. Ferreira, H. A. Pereira, S. I. Seleme and R. Teodorescu, “Reliability-Oriented Design of Modular Multilevel Converters for Medium-Voltage STATCOM,” in IEEE Transactions on Industrial Electronics, vol. 67, no. 8, pp. 6206-6214, Aug. 2020, doi: 10.1109/TIE.2019.2937050.

2. J. V. M. Farias, A. F. Cupertino, H. A. Pereira, S. I. Seleme and R. Teodorescu, “On Converter Fault Tolerance in MMC-HVDC Systems: A Comprehensive Survey,” in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 6, pp. 7459-7470, Dec. 2021, doi: 10.1109/JESTPE.2020.3032393.

3. D. C. Mendonça, R.O. de Sousa, J. V. M. Farias, H.A. Pereira, S. I. Seleme, A. F. Cupertino. Multilevel Converter for Static Synchronous Compensators: State-of-the-Art, Applications and Trends. Power Electronics for Green Energy Conversion. 1ed.: Wiley, 2022, p. 159-220. doi: 10.1002/9781119786511.ch6

4. J. V. M. Farias, L. -A. Grégoire, A. F. Cupertino, H. A. Pereira, S. I. Seleme and M. Fadel, ”A Sliding-Mode Observer for MMC-HVDC Systems: Fault-Tolerant Scheme With Reduced Number of Sensors,” in IEEE Transactions on Power Delivery, vol. 38, no. 2, pp. 867-876, April 2023, doi: 10.1109/TPWRD.2022.3200419.

The author also contributed to the following journal papers in the topic of modular multilevel cascaded converters:

1. P. R. Matias Jr, J. V. M. Farias, A. F. Cupertino, H. A. Pereira, M. M. Stopa and J. T. de Resende. "Redundancy and Derating Strategies for Modular Multilevel Converter for an Electric Drive." Journal of Control, Automation and Electrical Systems vol. 31, pp. 339–349, 2020. doi: 10.1007/s40313-019-00537-z.

2. P. R. Matias Jr, J. V. M. Farias, A. F. Cupertino, G. A. Mendonça, M. M. Stopa and H. A. Pereira. "Seleção da Tensão de Bloqueio Ótima de IGBTs para Inversores de Frequência Baseados em Conversor Modular Multinível." Revista Eletrônica de Potência vol. 25, no. 4, pp. 405-414, 2020. doi: 10.18618/REP.2020.4.0033.

3. J. V. G. França, J. H. D. G. Pinto, D. d. C. Mendonça, J. V. M. Farias, R. O. d. Sousa, H. A. Pereira, S. I. Seleme, A. F. Cupertino. Development of a Didactic Platform for Flexible Power Electronic Converters. Eletrônica de Potência (Impresso), v. 27, p. 225-235, 2022.

4. R. O. d. Sousa, A. F. Cupertino, J. V. M. Farias, et al. Modulation Strategy Impact on the Energy Storage Requirements of Modular Multilevel Converter-Based STATCOM. J Control Autom Electr Syst 34, 831–841 (2023). doi: 10.1007/s40313-023-01003-7

1.6 Ph.D Thesis Outline

This Ph.D thesis is organized in 6 chapters as follows. Chapter 2 describes the modeling, control and design of the MMC-based STATCOM. The topology, control strategy, main parameters and components design are detailed. Additionally, dynamic behavior of different semiconductor blocking voltages in an MMC-based STATCOM are evaluated in both experimental and simulation results. Chapter 3 presents a sliding-mode observer for MMC-based STATCOM employing only one current and one voltage measurement per MMC arm. In Chapter 4, the main proposed converter fault-tolerance schemes based on the available technical literature are described and critically compared. Moreover, the MMC dynamic performance during fault-tolerance operation is evaluated in both experimental and simulation results, while the observer is evaluated through simulations. In Chapter 5, the reliability-oriented design are presented. The best trade-off between cost and reliability is described considering MMC solutions of four different semiconductor blocking voltages and four different converter fault-tolerance schemes. Finally, the conclusions of this work are stated in Chapter 6.

2 MMC: Modeling, Control and Design

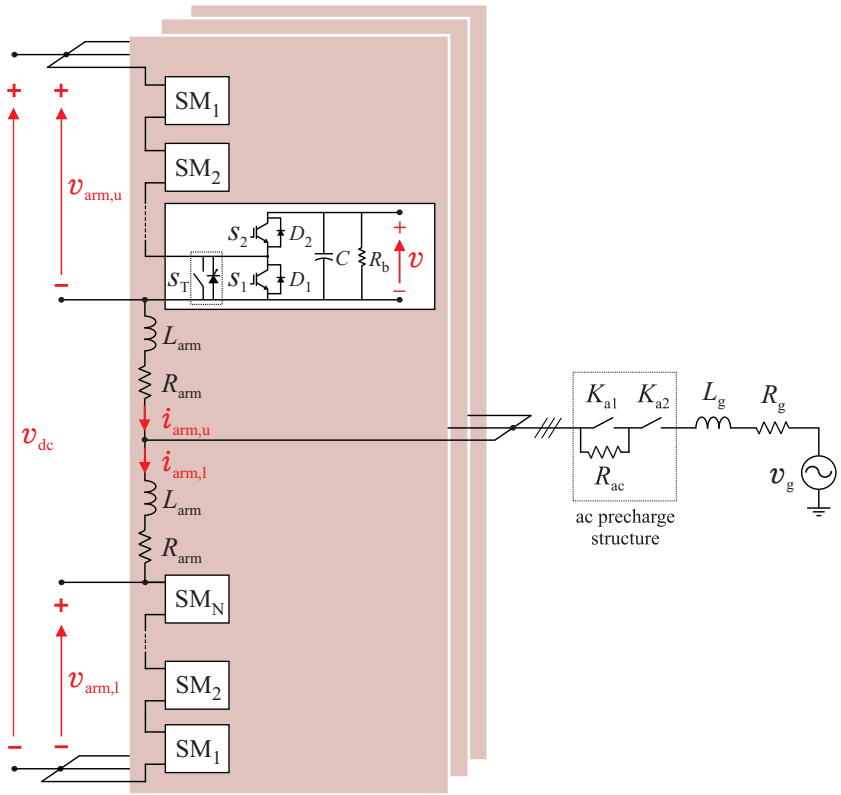
This chapter presents the topology, control and the main parameters design of the three-phase MMC-based STATCOM. A case study considering 17 MVA/13.8 kV MMC-based STATCOM is conducted aiming to evaluate the dynamic response of the converter.

2.1 Topology and Control Design

2.1.1 MMC Fundamentals

The schematic of the three-phase HB-MMC is presented in Fig. 15. The converter is composed of three legs, each one containing an upper and a lower arm. Each HB-MMC arm is composed of an arm inductor L_{arm}, an arm inductor resistance R_{arm} and N SMs. All SMs consist of two IGBTs S_1 and S_2, two antiparallel connected diodes D_1 and D_2, where it contains half the number of devices present in FB-SM, justifying the choice for HB-SM. Also, a capacitor C is presented in the SM. Generally, there is a bypass switch

Figure 15 – Schematic of the three-phase MMC-based STATCOM.



Source: Elaborated by the author.

S_T in parallel with each SM, which is usually composed by a thyristor in parallel with a vacuum contactor. In case of an SM failure, S_T bypasses the faulty SM (Gemmell et al., 2008). R_b represents the bleeder resistor, responsible for discharging the SM capacitor when the converter is turned off. Moreover, the inrush current is limited by ac-side charging resistances R_{ac} during pre-charge operation (de Sousa et al., 2020). The pre-charge is controlled by circuit breakers K_{a1} and K_{a2}. The converter is connected to the grid through a grid inductance L_g and inductor resistance R_g. The grid inductance also includes the leakage inductance of the isolation transformer used when galvanic isolation is required.

Figure 16 (a) illustrates a typical HB-SM, which can be switched in three different ways:

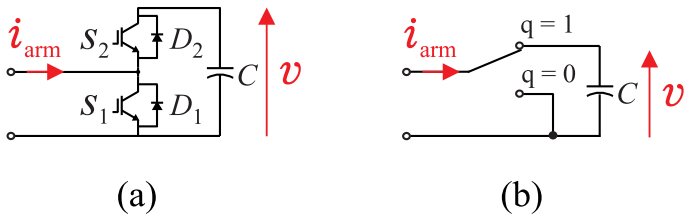
- **Inserted:** S_2 is turned on and S_1 is turned off. The SM capacitor is inserted in the arm circuit, allowing the capacitor to charge or discharge, depending on the direction of the arm current.
- **Bypassed:** S_1 is turned on and S_2 is turned off. The SM capacitor becomes bypassed and its voltage remains constant regardless of the arm current, since the bleeder resistor is neglected.
- **Blocked:** S_1 and S_2 are both turned off. In this operating mode the capacitor can charge through the diode of S_2, but it cannot discharge. This mode is used for energization of the converter. In addition, it may also be used during short time periods (typically tens of milliseconds or less) to protect the transistor from overcurrent, when dc-link faults occur.

During the energization of the converter, a positive arm current charges the SM capacitor through the anti-parallel diode D_2. A negative arm current polarizes the lower anti-parallel diode D_1, bypassing the SM. This converter operation is the well-known natural rectifying mode (NRM). For the normal MMC operation in controlled mode (CM), either the upper or the lower switch (including antiparallel diode) carries the arm current. In this sense, the two switches can be replaced by an ideal single switch, as shown in Fig. 16 (b). Therefore, the instantaneous voltage of a generic MMC arm can be described by:

$$v_{arm} = \sum_{n=1}^{N} q_n v_n, \tag{2.1}$$

where v_n are the instantaneous voltages of the n-th SM capacitor and q_n are the gate signals applied to the n-th SM upper-switch (S_2). In the HB-MMC, the gate signals $q_n \in \{0,1\}$ determine the SM states, as well as the insertion of the SM capacitors into the MMC arm.

Figure 16 – Possible representation of an SM-HB: (a) IGBT with antiparallel diode model; (b) Idealized model.



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A mathematical model can be obtained to define the main variables which describe the MMC dynamics. The most common approach for modeling static converters consists of equivalent circuits resulting from the different operating states, weighting the responses by the percentage of time that each one is active. However, this approach becomes impractical to MMC due to the large number of possible operating states. Therefore, a common procedure found in the literature is to find an equivalent non-switched circuit for the MMC arms, which allows to analyze the MMC dynamics (Antonopoulos; Angquist; Nee, 2009). In this sense, the converter presented in Fig. 15 can be modeled as shown in Fig. 17 (a), since the following assumptions are defined:

- The effect of the switching frequency is neglected;
- The SM capacitor voltages are assumed to be perfectly balanced.

The voltage sources represent the voltages synthesized by each arm, which can be assumed as continuous variables. According to the aforementioned assumptions, (2.1) can be rewritten as:

$$v_{arm} = v \sum_{n=1}^{N} g_n, \tag{2.2}$$

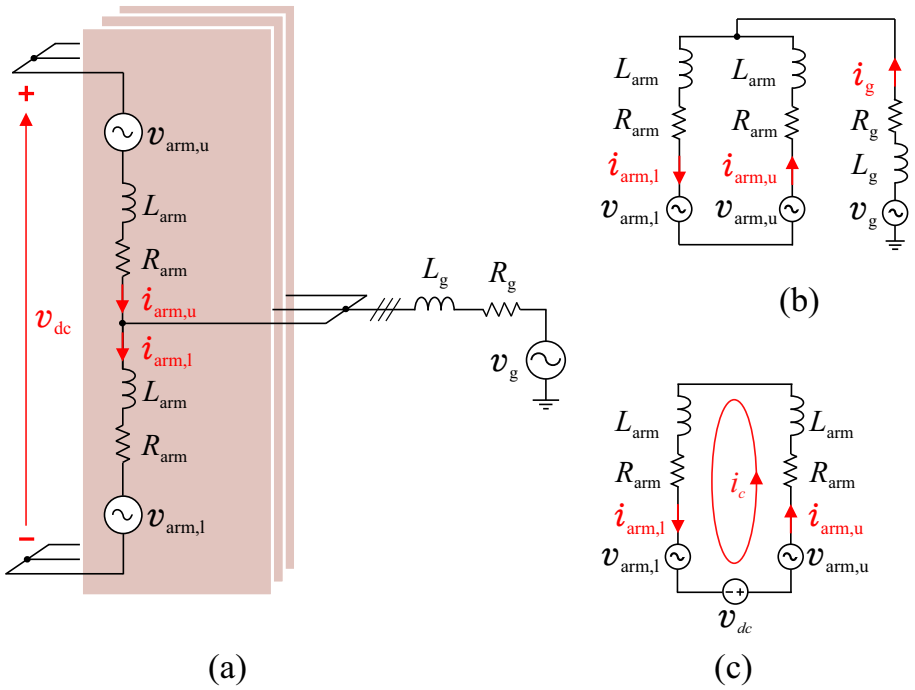
where g_n are the n-th SM duty cycles of the upper or lower arm, which provides the fraction of the switching period (T_c) when the capacitor is inserted into the MMC arm. The SM duty cycles are described as:

$$g_n = \frac{1}{T_c} \int_{t-T_c}^{t} q_n(\tau) d\tau. \tag{2.3}$$

Moreover, v is the average capacitor voltage values in the switching interval, given by:

$$v = \int_{t-T_c}^{t} v(\tau) d\tau. \tag{2.4}$$

Figure 17 – Schematic of the three-phase MMC-based STATCOM: (a) Average model; (b) Equivalent circuit describing the output current dynamics; (c) Equivalent circuit describing the circulating current dynamics.



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Since the non-switched circuit for the MMC arms are defined, the dynamics of the output and circulating currents can be obtained. The output current per phase is derived from Fig. 17 (b), based on Millman's theorem (Millman, 1940), as follows:

$$v_s + \left(\frac{1}{2}L_{arm} + L_g\right)\frac{di_g}{dt} + \left(\frac{1}{2}R_{arm} + R_g\right)i_g = v_g, \tag{2.5}$$

where v_g is the grid instantaneous line-to-neutral voltage and i_g is the grid current. The factor 1/2 appears in the arm inductance due to the Millman's theorem. v_s is the line-to-neutral voltage synthesized by the STATCOM (also referred to as output or terminal voltage), given by:

$$v_s = \frac{1}{2}(-v_{arm,u} + v_{arm,l}), \tag{2.6}$$

where $v_{arm,u}$ and $v_{arm,l}$ are the upper and lower arm voltages, respectively. The circulating current is an inherent characteristic of MMC and can occur when the voltages across different SMs are not perfectly balanced or due to the modulation strategy that causes the converter arms to switch at different times. The circulating current can be broken down into dc and ac components. The dc circulating current refers to the component of circulating current that flows through the dc-link of the MMC, while ac component of circulating current flows through the ac side of the MMC. In STATCOM operation, the

sum of the dc circulating current components across all phases remains zero, even though individual phases may exhibit dc values during unbalanced conditions. The circulating current dynamics can be obtained based on Fig. 17 (c), as follows:

$$\frac{v_{dc}}{2} - v_c = L_{arm}\frac{di_c}{dt} + R_{arm}i_c, \tag{2.7}$$

where v_c is the STATCOM internal voltage (which drives the circulating current) given by:

$$v_c = \frac{1}{2}(v_{arm,u} + v_{arm,l}), \tag{2.8}$$

and i_c is the converter circulating current giving by:

$$i_c = \frac{i_{arm,u} + i_{arm,l}}{2}. \tag{2.9}$$

where $i_{arm,u}$ and $i_{arm,l}$ are the upper and lower arm currents, respectively.

2.1.2 Control and Modulation Strategies

Since the output and circulating currents dynamics are defined through the MMC equivalent circuits, a proper control strategy must be employed to ensure the correct operation of the MMC-based STATCOM. The control strategy used in this work is presented in Fig. 18. The proposed grid (output) current control is responsible for injecting positive and negative sequence reactive power into the grid, as shown in Fig. 18 (a). The external loop controls the square of the average voltage v_{avg} of all converter SMs. The maximum number of "on-state" SMs in each arm during a fundamental period is equal to N. Under such conditions, the total number of operating SMs in the converter is $6N$. Therefore, the average voltage is computed by:

$$v_{avg} = \frac{1}{6N}\sum_{n=1}^{6N} v_n, \tag{2.10}$$

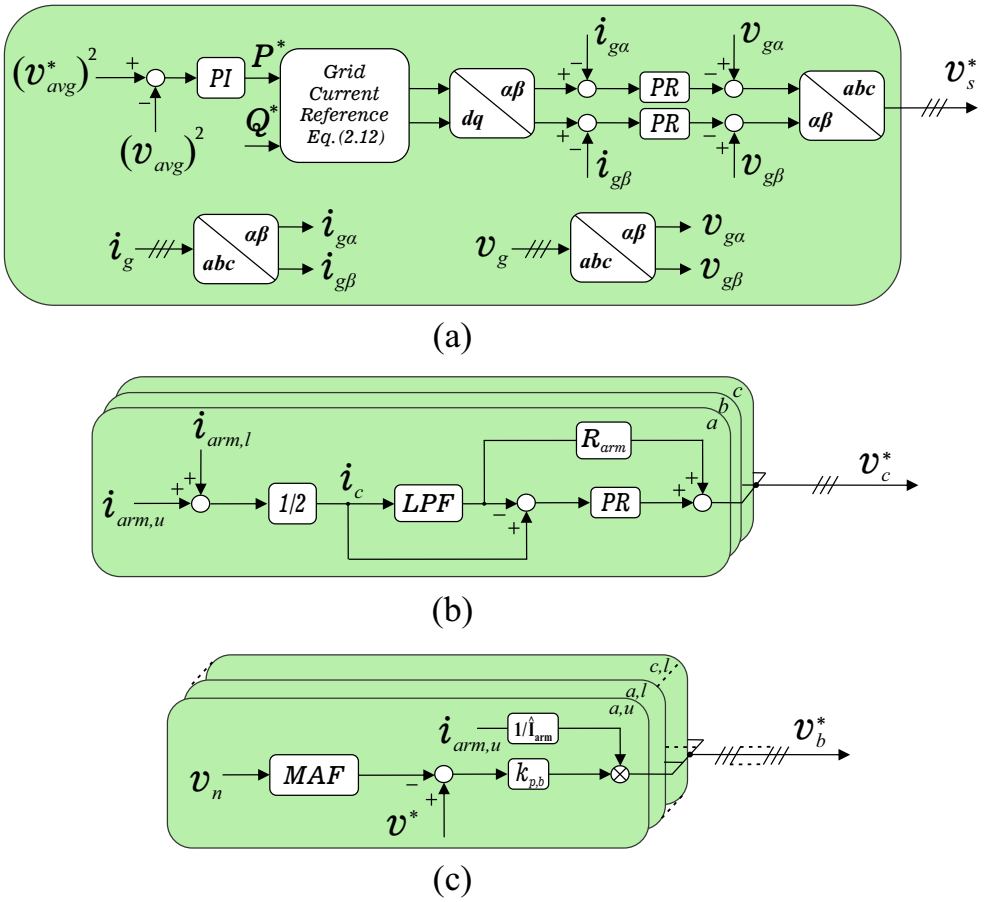
The average voltage reference v^*_{avg} is given by:

$$v^*_{avg} = \frac{V_{dc}}{N}, \tag{2.11}$$

where V_{dc} is the nominal MMC dc-link voltage.

The average voltage loop calculates the necessary active power P^* exchanged with the grid. Using the instantaneous power theory and assuming the a-axis of the three-phase grid voltage aligned to the d-axis of the dq-reference frame (Akagi; Watanabe; Aredes, 2007; Sharifabadi et al., 2016), the grid current in dq-reference frame can be computed by:

Figure 18 – Proposed control strategy for MMC-based STATCOM. (a) Grid current control; (b) Circulating current control; (c) Individual balancing control.



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$$i_{gd}^{*} = \frac{2}{3}\frac{P^{*}}{v_{gd}}, \qquad i_{gq}^{*} = -\frac{2}{3}\frac{Q^{*}}{v_{gd}}. \tag{2.12}$$

where v_{gd} is the d-direction grid voltage component and Q^{*} is the reactive power reference. The current control is implemented in stationary $\alpha\beta$-reference frame, converting the dq-reference frame from (2.12) to $\alpha\beta$-reference frame. Proportional resonant (PR) controllers are employed to track the reference output current $i_{g\alpha}^{*}$ and $i_{g\beta}^{*}$. Therefore, when small phase errors are present in the current control, steady-state errors appear in the active power, which is eliminated by the integral action of the dc-link voltage compensator.

The circulating current control reduces the harmonics and inserts damping in the converter dynamic response. Figure 18 (b) presents the circulating current control loop. As observed, this structure is implemented per MMC phase. A butterworth second-order low-pass filter is employed to remove the dc component of i_c. Furthermore, according to Xu et al. (2016), a considerable 2nd harmonic component is present in the circulating

current. This second order component generally cannot be compensated by the proportional controller (Yue et al., 2016). In view of this problem, a resonant controller tuned to the 2nd harmonic is added to the circulating current control.

An extra individual balancing control loop can be necessary to ensure the individual voltage balance of the SM capacitors, as observed in Fig. 18 (c). As suggested by Hagiwara and Akagi (2009), a proportional gain of the individual balancing controller $k_{p,b}$ is employed. In this case, the individual balancing control law is given by:

$$v_b^* = k_{p,b}(v^* - v_{f,n})\frac{i_{arm}}{\widehat{I}_{arm}}, \tag{2.13}$$

where v^* is the SM capacitor voltage reference. $v_{f,n}$ is obtained from the individual capacitor voltages through a moving average filter (Sasongko et al., 2016). The $\frac{i_{arm}}{\widehat{I}_{arm}}$ is proposed for real-time correction of the individual balancing control, instead of the sign(i_{arm}) function adopted in Hagiwara and Akagi (2009). Assuming the STATCOM operation under only positive sequence currents injection, $\widehat{I}_{arm} = \frac{\widehat{I}_g}{2}$ can be considered. It is important to remark that some modulation techniques ensure the voltage balance through the sorting and selection methods (Ghetti et al., 2017). In this work, no sorting and selection algorithm is used and the control loop indicated in Fig. 18 (c) is adopted.

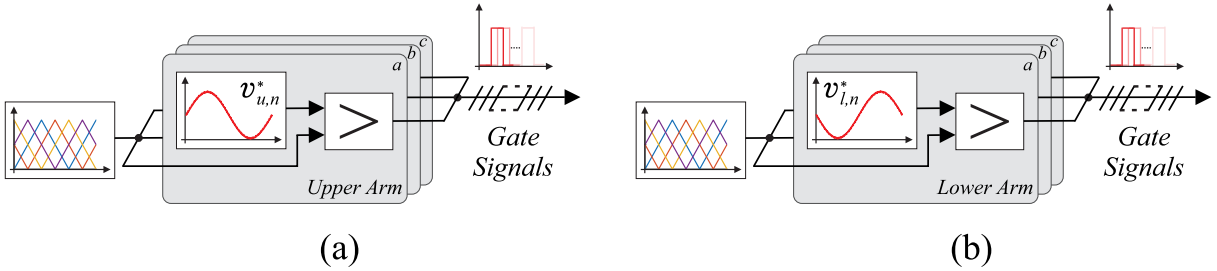
The reference signals depend on v_s^*, v_c^* and v_b^*, shown in Fig. 18. Under such conditions, the normalized reference signals per phase are given by (Farias et al., 2018):

$$v_{u,n}^* = \frac{v_b^*}{v^*} + \frac{v_c^*}{Nv^*} - \frac{v_s^*}{Nv^*} + \frac{1}{2}, \tag{2.14}$$

$$v_{l,n}^* = \frac{v_b^*}{v^*} + \frac{v_c^*}{Nv^*} + \frac{v_s^*}{Nv^*} + \frac{1}{2}. \tag{2.15}$$

Regarding the modulation strategy, the phase-shift carrier pulse width modulation (PSC-PWM) method is employed in this work, since STATCOM applications usually require moderate number of SMs per arm. The PSC-PWM consists of comparing the

Figure 19 – Block diagram of the PS-PWM modulation method for HB-MMC: (a) Upper arm; (b) Lower arm.



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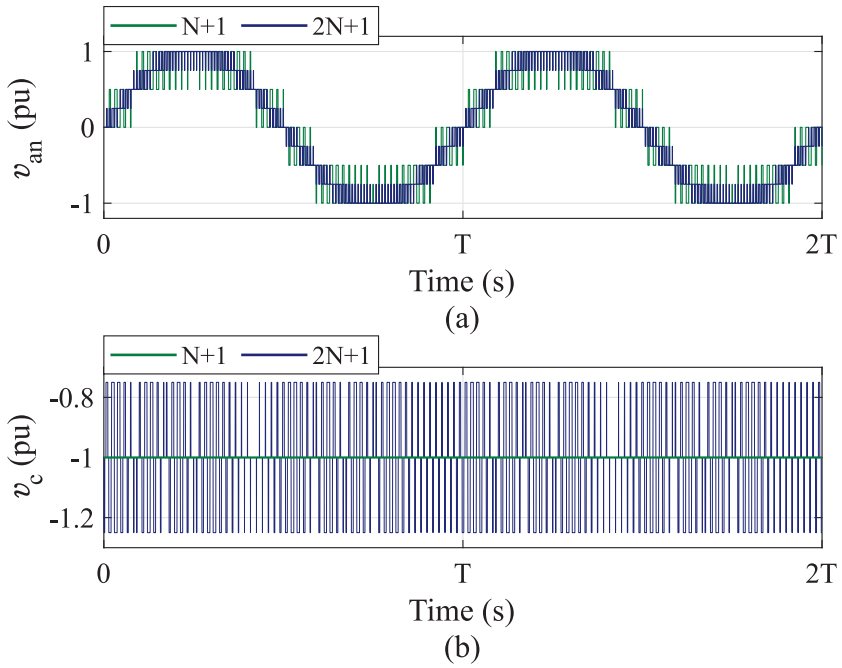
carriers with the reference voltage, generating the gate signals, as illustrated in Fig. 19. In the HB-MMC the angular displacement of the carriers is calculated according to the number of SMs, as follows:

$$\theta_{u,n} = 2\pi\left(\frac{i-1}{N}\right) \tag{2.16}$$

$$\theta_{l,n} = \theta_{u,n} + \beta_c, \tag{2.17}$$

where $i = 1, 2, ..., N$. The angle β_c indicates the phase displacement between the carrier waveforms in the upper and lower arms. The phase displacement of the carrier waveforms can be chosen in terms of the desired harmonic performance (Ilves et al., 2013). According to the phase displacement, $(N+1)$- or $(2N+1)$-level modulation strategies can be employed. Figure 20 (a) shows the HB-MMC phase voltage assuming 4 SMs per arm. As observed, the phase voltage has more levels in the $(2N+1)$-level modulation. This fact provides to the $(2N+1)$-level modulation a superior performance in terms of power quality at the ac side. Moreover, Figure 20 (b) shows that the $(2N+1)$-level modulation presents harmonic content in the internal voltage. Therefore, the number of inserted SMs in the upper and lower arms are not the same, which results in a higher circulating current ripple. Since in STATCOM applications the ac side power quality is preferred, the $(2N+1)$-level modulation is employed in this work (Sasongko et al., 2016). In this case, the phase displacement is given by:

Figure 20 – HB-MMC comparison of $(N+1)$- and $(2N+1)$-level phase-shifted modulation schemes: (a) Line-to-neutral voltage v_{an}; (b) Internal voltage v_c. *Remark*: N = 4 SMs per arm. Base value: V_{dc}



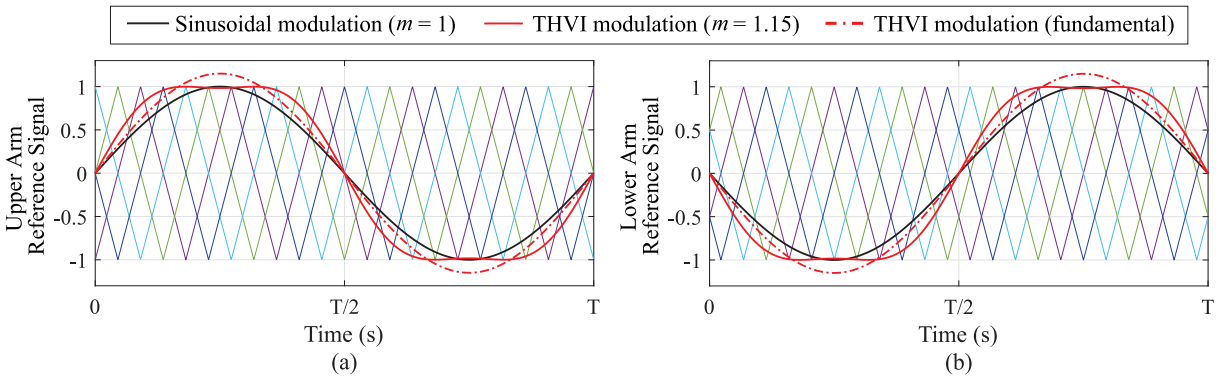
Source: Elaborated by the author.

$$\beta_c = 0, \quad \text{if N is odd} \tag{2.18}$$

$$\beta_c = \frac{\pi}{N}, \quad \text{if N is even} \tag{2.19}$$

Aiming to increase the linear operational area of the modulation curve in the sinusoidal PSC-PWM, the third harmonic voltage injection (THVI) method can be employed (Ilves et al., 2014). The carrier signals and the reference voltage normalized for both sinusoidal and 1/6 of THVI are shown in Fig. 21. As observed, the upper and lower arm reference voltages are 180° out of phase. In addition, the modulation index ($m = 2\widehat{V}_{sn}/V_{dc}$) can be increased by about 15% considering the THVI method. It is worth mentioning that THVI can be employed in MMC projects, as in the DolWin 3 project carried out by General Electric (GE, 2019). Moreover, power converters are usually implemented with THVI even under unbalanced grid conditions (Chen et al., 2015).

Figure 21 – PSC-PWM for HB-MMC with and without the injection of 1/6 of third harmonic. (a) Upper arm; (b) Lower arm. *Remark*: N = 4 SMs per arm and the maximum modulation index are adopted.



Source: Elaborated by the author.

Thus, when the THVI is inserted in the modulation, the normalized reference signals per phase (2.15) can be rewritten as:

$$v^*_{u,n} = \frac{v^*_b}{v^*} + \frac{v^*_c}{Nv^*} - \frac{v^*_s}{Nv^*} + \frac{v^*_{3s}}{Nv^*} + \frac{1}{2}, \tag{2.20}$$

$$v^*_{l,n} = \frac{v^*_b}{v^*} + \frac{v^*_c}{Nv^*} + \frac{v^*_s}{Nv^*} - \frac{v^*_{3s}}{Nv^*} + \frac{1}{2}. \tag{2.21}$$

where v^*_{3s} is 1/6 of third harmonic of the phase voltage reference. Finally, the control tuning is presented in detail in Appendix A.

2.1.3 Control under Unbalanced Grid Faults

The presence of HVDC stations is increasing in countries with significant use of wind energy, such as Germany, Denmark, United Kingdom, Spain and Ireland. According

to some grid codes, such stations are required to remain connected for a specified duration (Jia; Yang; Nielsen, 2018), typically at least 150 milliseconds, both during balanced and unbalanced grid faults. In such conditions, the injection of positives sequence reactive current during the fault for supporting the voltage recovery is expected. Additionally, the modern grid codes for renewable energy power plants require negative sequence support during voltage sags (VDE, 2015). It is important to remark that the so-called LVRT requirement are strictly related to the grid codes. Considering VDE (2015) for analysis, the requirements include:

- Prevent tripping of the converter, which can be due to output overcurrent or dc overvoltage.
- Inject (capacitive) positive sequence reactive current (2.22) proportional to the positive sequence voltage drop (as shown in Fig. 12 (a)):
- Inject (inductive) negative sequence reactive current (2.23) proportional to the negative sequence voltage (as shown in Fig. 12 (b)):

$$I_{q^+} = k_+(0.9 - V^+), \tag{2.22}$$
$$I_{q^-} = -k_-(V^- - 0.05). \tag{2.23}$$

where V^+ is the positive sequence voltage in pu. As highlighted in Fig. 12 (a), a $\pm 10\%$ non-injection band has been considered and the droop factor k_+ is considered to be (typically) 2.5 pu, which could be within the interval [0, 10] as requested by the local system operators. In the following, this requirement will be referred to as positive sequence injection low-voltage ride-through (PSI-LVRT). In addition, V^- is the negative sequence voltage in pu and a 5% non-injection band has been considered with droop factor k_-, which has the same considerations from k_+. Such requirement is observed in Fig. 12 (b) and is referred to as negative sequence injection low-voltage ride-through (NSI-LVRT).

Thus, during LVRT both positive and negative sequence reactive current have to be controlled independently. This requirement is challenging for the conventional control of the MMC illustrated in Fig. 18. Therefore, a mixed-sequence injection low-voltage ride-through (MSI-LVRT) (i.e. PSI and NSI simultaneously) is employed in this work (Sharifabadi et al., 2016). The objective of this approach is to introduce positive active current to maintain the load, positive reactive current in accordance with PSI-LVRT, and negative sequence reactive currents in accordance with NSI-LVRT. Consequently, the comprehensive reference for the MSI injection strategy case, according to Eqs. (2.12),(2.22) and (2.23), is as follows (Sharifabadi et al., 2016):

$$i^*_{gd^+} = \frac{2}{3}\frac{P^*}{v^+_{gd}}, \tag{2.24}$$

$$i^*_{gq^+} = k_+\left(0.9 - \frac{v^+_{gd}}{\widehat{V}_g}\right)\widehat{I}_g, \tag{2.25}$$

$$i^*_{gd^-} = 0, \tag{2.26}$$

$$i^*_{gq^-} = -k_-\left(\frac{v^-_{gd}}{\widehat{V}_g} - 0.05\right)\widehat{I}_g. \tag{2.27}$$

where v^+_{gd} and v^-_{gd} are the positive and negative sequence d-components of grid voltage, obtained through decoupled double synchronous reference frame based on positive negative sequence extraction (DDSRF-PNSE) with decoupling network (Teodorescu; Liserre; Rodriguez, 2007). Therefore, $i^*_{g\alpha\beta^+}$ and $i^*_{g\alpha\beta^-}$ can be obtained by the $dq-\alpha\beta$ transformation for each sequence. Finally, the following control description on Fig. 18 can be maintained, since $i^*_{g\alpha\beta}$ are evaluated by the direct sums of the positive and negative components, which is inherent characteristic of the stationary reference frame $\alpha\beta$.

Although such solution ensures compliance with both PSI-LVRT and NSI-LVRT, the instantaneous value of the MMC output currents may be different from phase to phase in some cases. In that way, accurate control of the power converter is necessary in order to avoid an undesired trip, since an overcurrent in any of the phases of the power converter usually results in the instantaneous disconnection of the converter from the grid. From the technical requirements in Germany, droop factors k_+ and k_- can be changed in order to limit the current in converter. However, such factors are request by the system operator aiming to support the grid voltage dip and reduce the unbalanced grid voltages. In that way, current limiter should be designed within MMC controller to protect the converter from overcurrents. Considering that PSI-LVRT strategy is adopted, the current limiter is straightforward and the converter current limit I_{max} can be restricted by (Jia; Yang; Nielsen, 2018):

$$I_{max} = \sqrt{i_d^2 + i_q^2}. \tag{2.28}$$

Therefore, since reactive current injection takes the first priority during faults in STATCOM application, i_d can be determined by (2.28) once i_q is defined in accordance with the grid codes. However, the complexity of managing converter current limits increases when unbalanced currents are introduced. In such scenarios, it becomes crucial to restrict both positive and negative sequence currents in appropriate manners and this is closely related to the chosen control strategies. To effectively constrain the current in each individual phase, a detailed analysis of converter current limits is essential for each specific control strategy, as discussed in (Jia; Yang; Nielsen, 2018). In general, $max\{I_a, I_b, I_c\} = I_{max}$

should be accomplished, where the converter current limit can be selected as more than 1 pu as well.

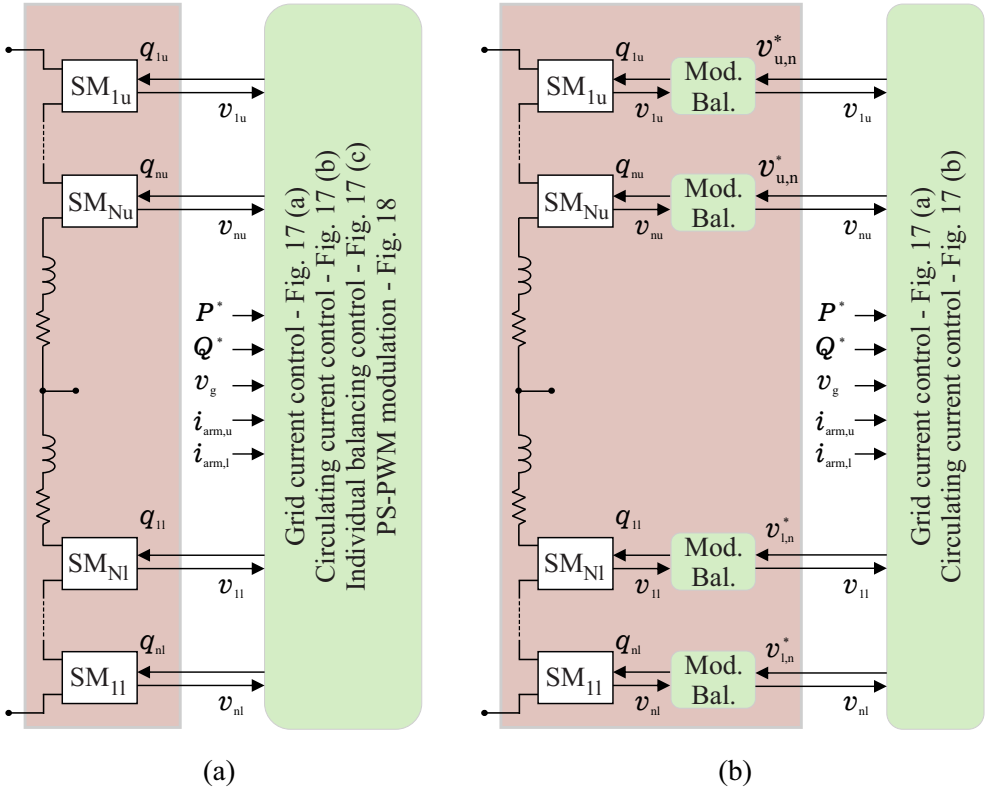
2.1.4 Control Architectures

Implementing an MMC control system can pose significant challenges due to the high number of SMs and the hierarchical control structure, as shown in Fig. 18. Such control arrangement can be effectively implemented through both centralized or decentralized architectures (Sharifabadi et al., 2016).

The centralized control architecture involves employing a single primary controller responsible for executing all essential processing and control tasks. Consequently, this approach places a substantial computational burden and required a high number of input/output units. Additionally, a considerable amount of fiber-optic cables is essential to establish connections between each SM and the central controller. This poses challenges in terms of cost and complexity. A conceptual representation of centralized control is depicted in Fig. 22 (a). For the sake of simplicity, only the main signals exchanged between the main controller and each SM of upper and lower arms in only one phase are displayed.

On the other hand, decentralized architecture involves multiple controllers with

Figure 22 – Conceptual MMC control architectures: (a) centralized (b) SM-level decentralized. *Remark:* only one MMC phase is illustrated.



Source: Adapted from Sharifabadi et al. (2016).

distinct structures. The specific decentralized architectures depend on how the controllers distribute tasks among themselves. For example, a decentralized structure (SM-level decentralized) can be applied for large MMC systems, where the arm is physically built in several sections, as illustrated in Fig. 22 (b). Each SM controller receives the voltage reference, where individually carries out PWM modulation and individual balancing control. It is important to remark that $v^*_{ul,n}$ is obtained from (2.15) disregarding the term v^*_b related to the individual balancing control, since such control will be done individually in each SM controller.

2.2 MMC-based STATCOM Design

2.2.1 Switching Frequency

In MMC applications, the switching and sampling frequencies should be carefully defined (Siddique et al., 2016). Since the HB-MMC topology and PSC-PWM modulation are employed, a total number of carriers required is $2N$. Therefore, the effective output frequency considering $(2N+1)$-level modulation is given by (Marzoughi; Burgos; Boroyevich, 2019):

$$f_{ef} = 2N f_c, \tag{2.29}$$

where f_c is the carrier frequency of each SM. The MMC is different from most other VSC topologies because a low switching frequency per device can be employed without sacrificing the quality of the output voltage waveform. Therefore, the switching frequency should be chosen to ensure low switching power losses as well as maintaining good transient performance and capacitor voltage balancing.

A suitable choice of f_c also should support the digital low-pass filter design (Sasongko et al., 2016). This filter attenuates the ac component included in SM capacitor voltages, which works as a disturbance in the current control system. According to the switching frequency employed, the digital low-pass filter must eliminate the first- and second-order supply frequency components, as well as the capacitor switching components. Therefore, assuming the digital low-pass filter as a moving-average filter, the window time is described by (Sasongko et al., 2016):

$$T_{ma} = \frac{1}{f_g}, \quad \text{if} \quad (f_c > 4f_g) \tag{2.30}$$

$$T_{ma} = \frac{f'_g}{f_g}, \quad \text{if} \quad (f_c \leq 4f_g) \tag{2.31}$$

where f_g' is obtained from the irreducible fraction of the carrier frequency f_c with respect to the supply frequency f_g, denoted by f_c'/f_g'. [1] Note that a relation of $f_c/f_g = f_c'/f_g'$ indicates that the carrier waveform is repeated f_c' times in the time interval given by multiplying the supply-frequency period by f_g'. From (2.31), setting f_g' to be lower makes the delay time caused by the moving-average filter shorter. Therefore, the smallest delay caused by the moving-average filter occurs by choosing f_c as an integer multiple of f_g. However, according to Ilves et al. (2015), the carrier frequencies integer multiple of the f_g may cause instability in the capacitor voltage balancing. Thus, an interesting value for the carrier frequency is given by:

$$f_c = \frac{x}{2} f_g, \tag{2.32}$$

where $x = \{3, 5, 7\}$, since $f_g \leq f_c \leq 4f_g$. In this work, $x = 7$ is adopted aiming to provide a suitable performance for the MMC dynamics without compromising the converter efficiency.

2.2.2 Current Ratings

2.2.2.1 Arm Currents

Expressions for the HB-MMC arm currents can be used to define the current of the semiconductor devices. Arm currents per phase can be expressed by:

$$i_{arm,u} = i_c - \frac{i_g}{2}, \tag{2.33}$$

$$i_{arm,l} = i_c + \frac{i_g}{2}. \tag{2.34}$$

Regarding STATCOM application, the control strategy needs to work during unbalanced conditions. Therefore, the assumed three-phase grid voltage is given by:

$$v_g = \widehat{V}_g^{+}\cos(\omega_g t + \delta^{+} + \theta_v) + \widehat{V}_g^{-}\cos(\omega_g t + \delta^{-} - \theta_v), \tag{2.35}$$

where $\widehat{V}_g^{+}$ and $\widehat{V}_g^{-}$ are the amplitudes of positive and negative sequence components of line voltage, respectively. Additionally, δ^{+} and δ^{-} are the positive and negative sequence voltage angles, respectively, which $\delta^{+} = 0$ is typically employed for the MMC phase A. Moreover, $\theta_v \in \{-\frac{2\pi}{3}, 0, \frac{2\pi}{3}\}$ refers to the phase angle of each phase and ω_g is the grid frequency. Since the MMC injects both positive and negative sequence currents, i_g is given by:

[1] For example, when $f_c = 210$ Hz and $f_g = 60$ Hz, $f_c'/f_g' = 7/2$. Therefore, $f_c' = 7$ and $f_g' = 2$. Thereby, $1/f_{ma} = 2/f_g$.

$$i_g = \widehat{I}_g^{+}\cos(\omega_g t + \phi^{+} + \theta_v) + \widehat{I}_g^{-}\cos(\omega_g t + \phi^{-} - \theta_v), \tag{2.36}$$

where $\widehat{I}_g^{+}$ and $\widehat{I}_g^{-}$ are the amplitudes of positive and negative sequence currents, respectively. Moreover, ϕ^{+} and ϕ^{-} are the positive and negative sequence current angles, respectively.

Considering that the harmonics in the circulating current are suppressed, its value can be given by (Yue et al., 2016):

$$\begin{aligned} i_c = \frac{\widehat{V}_g^{+}}{2V_{dc}}\left[\widehat{I}_g^{+}\cos(-\phi^{+}) + \widehat{I}_g^{-}\cos(-\phi^{-} - \theta_v)\right] \\ + \frac{\widehat{V}_g^{-}}{2V_{dc}}\left[\widehat{I}_g^{+}\cos(\delta^{-} - \phi^{+} + \theta_v) + \widehat{I}_g^{-}\cos(\delta^{-} - \phi^{-})\right], \end{aligned} \tag{2.37}$$

Due to symmetry, only the lower arm current is verified. The maximum value for the current can be obtained by (2.33) as:

$$\max(i_{arm,l}) = \max(i_c) + \frac{1}{2}\max(i_g). \tag{2.38}$$

For simplification, the negative sequence voltage synthesized by the converter is considered much smaller than the synthesized positive sequence. Moreover, the MMC arm current limit is the same even considering both positive sequence or negative sequence current as presented in Cupertino et al. (2019a). In that way, $\max(i_c) \leq \frac{1}{4} m_{max}\widehat{I}_g$ and $\max(i_g) \leq \widehat{I}_g$, where m_{max} is the maximum modulation index and $\widehat{I}_g$ is given by:

$$\widehat{I}_g = \frac{\sqrt{2}}{\sqrt{3}}\frac{S_n}{V_g}. \tag{2.39}$$

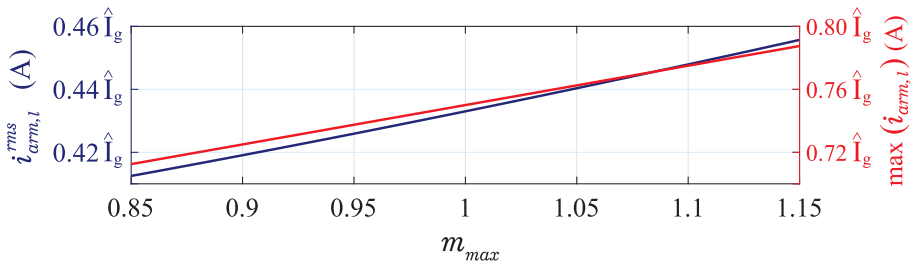
where V_g is the rms line-to-line voltage of the grid and S_n is the converter rated power. Thus, the maximum and rms lower arm current are:

$$\max(i_{arm,l}) = \left(\frac{1}{2} + \frac{m_{max}}{4}\right)\widehat{I}_g, \tag{2.40}$$

$$i_{arm,l}^{rms} = \frac{\widehat{I}_g}{2}\sqrt{\frac{(m_{max})^2}{4} + \frac{1}{2}}. \tag{2.41}$$

Figure 23 illustrates the maximum and rms lower arm current values as a function of the maximum modulation index. Furthermore, the maximum modulation index with the injection of 1/6 of third harmonic is $m_{max} = 1.15$. Under such conditions, the maximum and rms lower arm current values are $\max(i_{arm,l}) = 0.79\widehat{I}_g$ and $i_{arm,l}^{rms} = 0.46\widehat{I}_g$, respectively.

Figure 23 – Maximum and rms lower arm current values as a function of the maximum modulation index.



Source: Elaborated by the author.

2.2.3 Number of SMs

The minimum value of the dc-link voltage can be approximated by (Fujii; Schwarzer; De Doncker, 2005):

$$V_{dc} = \frac{2\sqrt{2}}{\sqrt{3}(1-\Delta V_{dc})}\frac{V_s}{m_{max}}, \tag{2.42}$$

where ΔV_{dc} is the dc-link voltage ripple. V_s is the rms line-to-line voltage synthesized by the STATCOM, described by (Fujii; Schwarzer; De Doncker, 2005):

$$V_s = (1+\Delta V_g)\left[1 + x_{eq,pu}\left(1+\Delta x_{eq}\right)\right] V_g, \tag{2.43}$$

where ΔV_g is the grid voltage variation, $x_{eq,pu}$ is the maximum per unit value of the output reactance and Δx_{eq} is the output reactance variation.

In that way, the number of SMs can be determined by:

$$N = \frac{1}{f_{us}}\frac{V_{dc}}{V_{svc}}, \tag{2.44}$$

where f_{us} is the device utilization factor defined by the ratio between the reference voltage of SMs v^* and the semiconductor device voltage class V_{svc}. Since the presence of a continuous dc voltage across the devices leads to a higher probability of cosmic ray failure or of thermal runaway, Table 4 indicates typical values for device utilization factor of ABB IGBT power module (ABB, 2017). As observed, the maximum recommended nominal voltage for semiconductor devices are below 60% of V_{svc} due to safety margins. Therefore, assuming an SM capacitor voltage ripple of up to 10%, $f_{us} = 50\%$ is defined. Under such conditions, the number of SMs per arm can be rewritten as:

$$N = \frac{2V_{dc}}{V_{svc}}, \tag{2.45}$$

Table 4 – IGBT modules specifications for HB-MMC (ABB, 2017).

$\mathbf{V}_{svc}$ (V)	$\mathbf{V}_{nom}$ (V)	$\mathbf{f}_{us}(\%)$
1700	900	52.94
3300	1800	54.55
4500	2250	50.00
6500	3600	55.38

2.2.4 SM Capacitance

Considering that all SM capacitor voltages are perfectly balanced, the instantaneous SM power of a generic MMC arm can be written as (Mendonça et al., 2022):

$$p_{sm} = \frac{v_{arm} i_{arm}}{N}, \tag{2.46}$$

Neglecting the SM power losses yields:

$$\frac{v_{arm} i_{arm}}{N} = v\left(C\frac{dv}{dt}\right) \approx V^*\left(C\frac{dv}{dt}\right), \tag{2.47}$$

where a small ripple is assumed. Under such conditions, the following expression can be obtained from (2.47):

$$v(t) = V^* + \frac{1}{NCV^*}\overbrace{\int v_{arm} i_{arm} dt}^{f(t)}. \tag{2.48}$$

As observed, expression (2.48) describes the SM capacitor voltage waveform. Usually, the capacitance is determined for a given voltage ripple requirement. The capacitor voltage ripple from average to peak (or valley) can be computed based on the maximum absolute value of the function $f(t)$. Accordingly:

$$\Delta V = \frac{\max(|f(t)|)}{NCV^*}. \tag{2.49}$$

Assuming $\Delta V = \delta V^*$, where δ is per unit (pu) voltage ripple, the SM capacitance can be estimated by:

$$C = \frac{\max(|f(t)|)}{N\delta V^{*2}}. \tag{2.50}$$

The maximum output voltage in HB-MMC is obtained when all SMs are inserted with positive voltage. In this analysis, only positive sequence current is considered. Therefore, the circulating current is assumed to be zero. Moreover, it is assumed that the voltage required to control the circulating current is very low. It is important to remark

that the peak value of the arm current is obtained from (2.40), where $\max(i_{arm}) < \widehat{I}_g$, aiming to ensure safe operation of the converter. Therefore, the negative sequence current required in the converter during LVRT, which is strictly related to grid codes, can be neglected without considerably affecting the design of the SM capacitors. This statement is well demonstrated by simulation results in Section 2.3.1.4.

Based on the previous assumptions, $f(t)$ for HB-MMC is given by:

$$f(t) = \int \left(\widehat{V}_{sn} - \widehat{V}_{sn}\cos\left(\omega_g t\right)\right) \frac{\widehat{I}_g}{2}\cos\left(\omega_g t + \phi^+\right) dt \tag{2.51}$$

$$= \frac{\widehat{V}_{sn}\widehat{I}_g}{\omega_g} \overbrace{\left[\frac{1}{2}\sin\left(\omega_g t + \phi^+\right) - \frac{1}{8}\sin\left(2\omega_g t + \phi^+\right)\right]}^{f_1(t)}. \tag{2.52}$$

where $\widehat{V}_{sn}$ is the peak value of the phase voltage synthesized by the MMC. In the STATCOM operation mode, the phase difference between grid voltage and current is equal to $\phi^+ = \pm\frac{\pi}{2}$. By inspection, the maximum absolute value of $f_1(t)$ is $\frac{5}{8}$, which is illustrated in Fig. 24 (a). Therefore,

$$\max(|f(t)|) = \frac{5}{8}\frac{\widehat{V}_{sn}\widehat{I}_g}{\omega_g}. \tag{2.53}$$

Substituting (2.53) in (2.50) yields:

$$C = \frac{5}{8}\frac{\widehat{V}_{sn}\widehat{I}_g}{\omega_g N \delta V^{*2}}. \tag{2.54}$$

Assuming $x_{eq,pu} = 0.2$ and no variation in grid voltage and output reactance, the peak value of the phase voltage $\widehat{V}_{gn}$ can be obtained by (2.43) for $\widehat{V}_{sn} = 1.2\widehat{V}_{gn}$. In addition, since the converter only processes reactive power, the three-phase reactive power is:

$$Q_n = \frac{3}{2}\widehat{V}_{gn}\widehat{I}_g. \tag{2.55}$$

Replacing (2.55) in (2.54) yields:

$$C = \frac{1}{2}\frac{Q_n}{\omega_g N \delta V^{*2}}. \tag{2.56}$$

The analysis previously performed for HB-MMC is valid only for sinusoidal modulation in the limit of the linear region of the modulator. When 1/6 of THVI is employed, $f(t)$ is given by:

$$f(t) = \int \left(\frac{\sqrt{3}}{2}\widehat{V}_{sn} - \widehat{V}_{sn}\cos\left(\omega_g t\right) + \frac{\widehat{V}_{sn}}{6}\cos\left(3\omega_g t\right) \right) \frac{\widehat{I}_g}{2}\cos\left(\omega_g t + \phi^+\right) dt$$

$$= \frac{\widehat{V}_{sn}\widehat{I}_g}{\omega_g} \overbrace{\left[\frac{\sqrt{3}}{4}\sin\left(\omega_g t + \phi^+\right) - \frac{1}{8}\sin\left(2\omega_g t + \phi^+\right) + \frac{1}{96}\sin\left(4\omega_g t + \phi^+\right) + \frac{1}{48}\sin\left(2\omega_g t - \phi^+\right) \right]}^{f_2(t)} \tag{2.57}$$

By inspection, the maximum absolute value of $f_2(t)$ is $\frac{24\sqrt{3}+13}{96}$, which is illustrated in Fig. 24 (b). Thus,

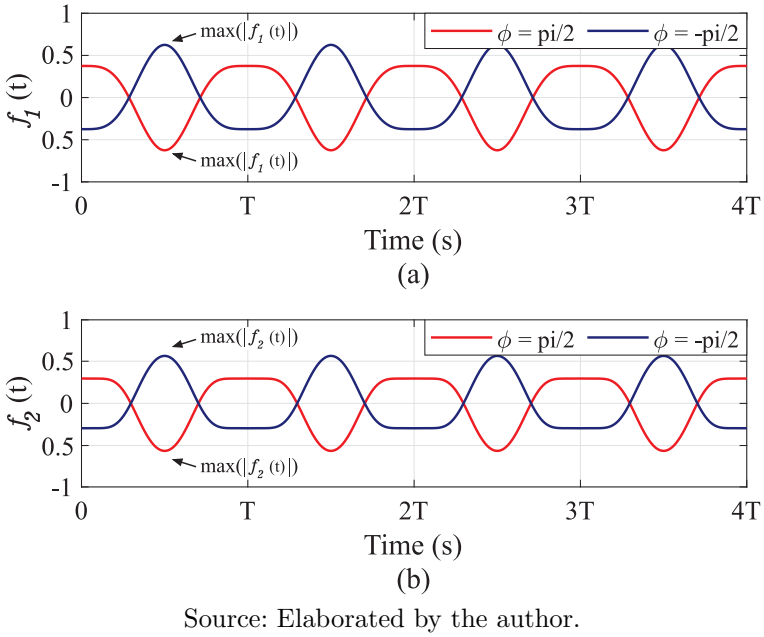
$$\max(|f(t)|) = \frac{24\sqrt{3}+13}{96}\frac{\widehat{V}_{sn}\widehat{I}_g}{\omega_g}. \tag{2.58}$$

Assuming the same considerations aforementioned, the SM capacitance when 1/6 of THVI is employed can be described as:

$$C = \frac{24\sqrt{3}+13}{120}\frac{Q_n}{\omega_g N \delta V^{*2}}. \tag{2.59}$$

From (2.56) and (2.59), the SM capacitance is reduced of around 10%, which causes an expected reduction in the energy storage requirement. It is important to remark that the variation in the dc-link voltage and the number of SMs N are neglected. Additionally, the spreading effect, which quantifies the difference between the capacitor voltages and

Figure 24 – The normalized ac component of the SM capacitor voltages of HB-MMC. (a) Sinusoidal PWM; (b) THVI-PWM.



Source: Elaborated by the author.

the average value, in the SM capacitor voltages can be affected according to the adopted modulation strategy (de Sousa et al., 2023), while this work is only focusing in the PS-PWM method.

2.2.5 Arm Inductance

Regarding the arm inductance, some papers present methodologies based on HB-MMC circulating current. Once the control strategy suppresses the second harmonic component of the circulating current, the following relationship must be satisfied to prevent the resonance frequency between the arm inductor and the SM capacitors (Ilves et al., 2012):

$$L_{arm}C > \frac{5N}{48\omega_g^2}. \tag{2.60}$$

Another feature performed by the inductor is to limit the arm current during faults (Xu; Xiao; Zhang, 2016). Considering a short circuit applied between the positive and negative dc-buses, the arm inductance which limits the fault current is calculated by:

$$L_{arm} = \frac{V_{dc}}{2\alpha_r}, \tag{2.61}$$

where α_r (kA/s) is the maximum current rise rate.

The arm inductance is also responsible for improving the circulating current performance. Considering PSC-PWM modulation and $(2N+1)$-level modulation, the arm inductance can be derived to limit the peak-to-peak circulating current ripple Δi_c as follow (Li; Jones; Wang, 2017):

$$L_{arm} = \frac{3}{32C\omega_g f_c}\frac{\widehat{I}_g}{\Delta i_c}, \tag{2.62}$$

The criteria from (2.60) is usually satisfied, since the minimum required arm inductance is below the other criteria presented. Moreover, (2.61) is normally required only when a connection is presented in the common dc-link to limit the arm current during dc faults. In that way, (2.62) is adopted to calculate the MMC arm inductance in this work.

2.3 Results

This section aims to validate the proposed methodology in terms of dynamics and steady-state performances of the HB-MMC, operating during both positive and negative sequences injection. The simulations were performed in PLECS environment based on the

topology presented in Fig. 15. Experimental results in a downscaled MMC prototype are also obtained to validate the control strategy employed.

2.3.1 Simulation Results

2.3.1.1 Parameter Setting

A 17 MVA MMC-STATCOM with rms line-to-line voltage (V_g) of 13.8 kV is considered. Moreover, a dc-link voltage of $V_{dc} = 25$ kV is adopted. Table 5 presents the main circuit parameters based on the methodology described above. Commercially available IGBTs with blocking voltage capability of 1.7, 3.3, 4.5 and 6.5 kV are employed, aiming to evaluate different HB-MMC designs (i.e. C_{17}, C_{33}, C_{45} and C_{65}).

The arm inductors are designed to satisfy the above constraint and to limit the total harmonic distortion (THD) in the output current i_g below 5% (IEEE, 2014). Moreover, 4% of the maximum peak-to-peak circulating current ripple is applied. The arm resistances are computed considering the typical arm inductor X/R ratio of 40. The grid impedance are chosen as 0.05 pu. Furthermore, grid X/R ratio of 18 is employed for all cases. Finally, the bleeder resistors are chosen to ensure a discharge of the SM capacitor at $5\tau = 180s$, where $\tau = R_b C$.

The controller frequencies are evaluated as function of the sampling frequency $f_s = f_{ef}$. Therefore, the controller parameters are shown in Tab. 6. The proportional integral controllers are discretized by Tustin method, while the proportional resonant controllers are discretized by Tustin with prewarping method.

Table 5 – Main parameters of the MMC for four proposed designs for simulation results.

Parameter		**MMC specifications**			
		C_{17}	C_{33}	C_{45}	C_{65}
N		29	15	11	7
V_{svc}	(kV)	1.7	3.3	4.5	6.5
V^*	(kV)	0.86	1.67	2.27	3.57
f_{us}	(%)	51	51	51	55
$I_{arm,rms}$	(A)	460	460	460	460
$\widehat{I}_{arm}$	(A)	788	788	788	788
C	(mF)	9.51	4.92	3.61	2.30
L_{arm}	(mH)	3.11	6.02	8.20	12.89
R_{arm}	(Ω)	0.03	0.06	0.08	0.12
L_g	(mH)	1.5	1.5	1.5	1.5
R_g	(Ω)	0.03	0.03	0.03	0.03
R_{ac}	(Ω)	25	25	25	25
R_b	(kΩ)	3.78	7.32	9.97	15.68
f_c	(Hz)	210	210	210	210
f_{ef}	(kHz)	12.18	6.30	5.62	2.94

Table 6 – MMC-based STATCOM parameters of the controller for simulation results.

Parameter	$\mathbf{C}_{17}$	$\mathbf{C}_{33}$	$\mathbf{C}_{45}$	$\mathbf{C}_{65}$
Proportional gain of average control $k_{p,v}$ (Ω^-1)	45.7	12.2	6.6	2.7
Integral gain of average control $k_{i,v}$ (Ω^-1/s)	209	55.9	30.1	12.2
Proportional gain of grid current control $k_{p,g}$ (Ω)	23.4	17.9	16.3	14.7
Resonant gain of grid current control $k_{r,g}$ (Ω/s)	8814	6730	6128	5533
Proportional gain of circulating current control $k_{p,c}$ (Ω)	24	24	24	24
Resonant gain of circulating current control $k_{r,c}$ (Ω/s)	8980	8980	8980	8980
Integral gain of reactive power control $k_{i,q}$ (Ω^-1/s)	7.65	3.96	2.91	1.85
Proportional gain of individual balancing control $k_{p,b}$ (V^-1)	2.49	1.29	0.95	0.61
Circulating current LPF cut-off frequency (Hz)	8	8	8	8

2.3.1.2 HB-MMC energization

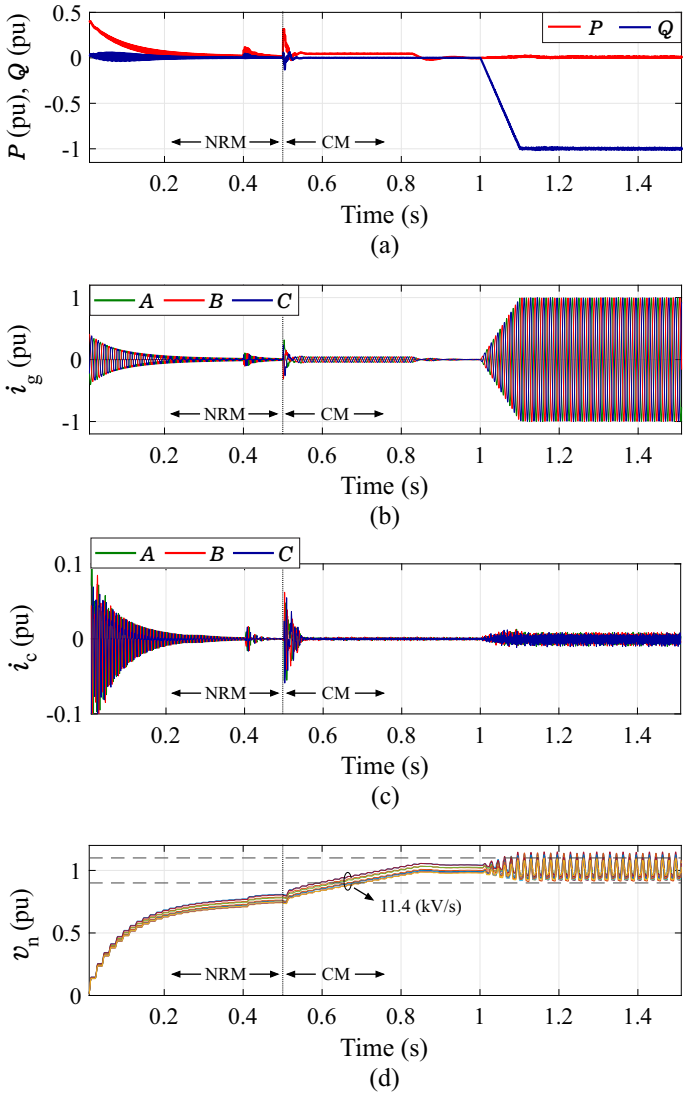
The charging resistors limit the in-rush current during the pre-charge operation in NRM until the converter operates in CM. These stages can be divided as follows:

- t = 0 s: the system is connected at the grid side. K_{a2} is closed and K_{a1} is opened;
- t = 0.4 s: removing the ac-side charging resistances. K_{a1} is closed;
- t = 0.5 s: enabling the closed-loop control;
- t = 1 s: enabling the ramp of -1700 Mvar/s during the converter capacitive operation.

For the sake of simplicity, the results shown are based on the C_{45} solution, which employs semiconductor blocking voltage of 4.5 kV. Moreover, all results are presented in pu in the base values illustrated in Tab. 5. Figure 25 (a) shows the reactive and active power flow. As noted, active power is absorbed from the grid during NRM, since the SM capacitors must be charged. When the ac-side charging resistances are removed in t = 0.4s, the amount of active power held by the resistors is forwarded to the capacitors, up to the charged limit defined in NRM. CM is started in t = 0.5s, where more active power is absorbed for charging the capacitors up to the rated voltage. After t = 1s, the converter is brought to the nominal operating condition reaching -1 pu of reactive power in capacitive operation. Moreover, the active power presents an average value less than 0.01 pu, which corresponds to the MMC power losses.

The grid and circulating currents are illustrated in Figs. 25 (b) and (c), respectively. As observed, the grid current is limited in NRM and tends to decrease, since, initially, the closed-loop control is disabled. After t = 1s, the grid current amplitude increases according to the reactive power reference in ramp with slope of -1700 Mvar/s. Similar behavior is observed in the circulating currents. As observed, the circulating currents present no dc value, since only reactive power is processed by the converter. In the nominal operating condition, the circulating currents are limited to values below 0.01 pu.

Figure 25 – Dynamic behavior of HB-MMC during energization condition: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents; (d) SM capacitor voltages.



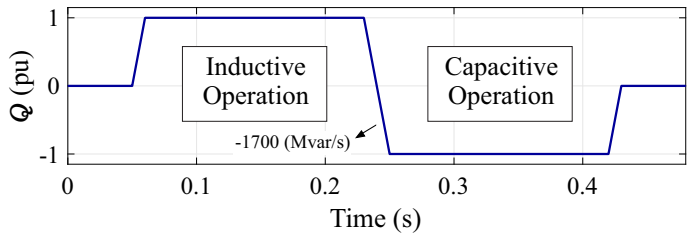
Source: Elaborated by the author.

The SM capacitor voltages are illustrated in Fig. 25 (d). Only the upper arm of MMC phase A is analyzed. Furthermore, the values of the SM capacitances are inserted into the model considering a tolerance of 10% with normal distribution. As observed, the SM capacitors are charged up to $\frac{\widehat{V}_g}{N}$, which is the limit value reaches in NRM by the ac-side pre-charge. During CM, the SM capacitors are charged up to V^* in ramp with slope 11.4 kV/s. Moreover, the SM capacitor voltages oscillate with 10% of ripple in nominal operating condition, as indicated by the dashed lines.

2.3.1.3 Positive Sequence Injection (PSI)

In this case study, only positive sequence injection is considered. Under such conditions, the trapezoidal reactive power profile presented in Fig. 26 is employed. The

Figure 26 – Reactive power profile considering both inductive and capacitive reactive power operations.



Source: Elaborated by the author.

aim is to verify if the performance of the capacitor voltage balancing and if the selected parameters are suitable when the converter operates in both inductive or capacitive mode.

The instantaneous active and reactive powers are presented in Fig. 27 (a). As observed, the reactive power exchanged follows the reference profile. Furthermore, the active power presents an average value less than 0.01 pu over the whole profile, which corresponds to the MMC power losses. The grid currents shown in Fig. 27 (b) follow the shape of the reactive power profile. Additionally, the grid current THD in both operations is less than 3%, which meets the THD limit of 5% (IEEE, 2014). Furthermore, the circulating currents are presented in Fig. 27 (c). As noted, the circulating current ripple is below 2% during steady state, as specified at the design stage. Moreover, the second harmonic component in i_c is almost fully compensated by the control strategy employed.

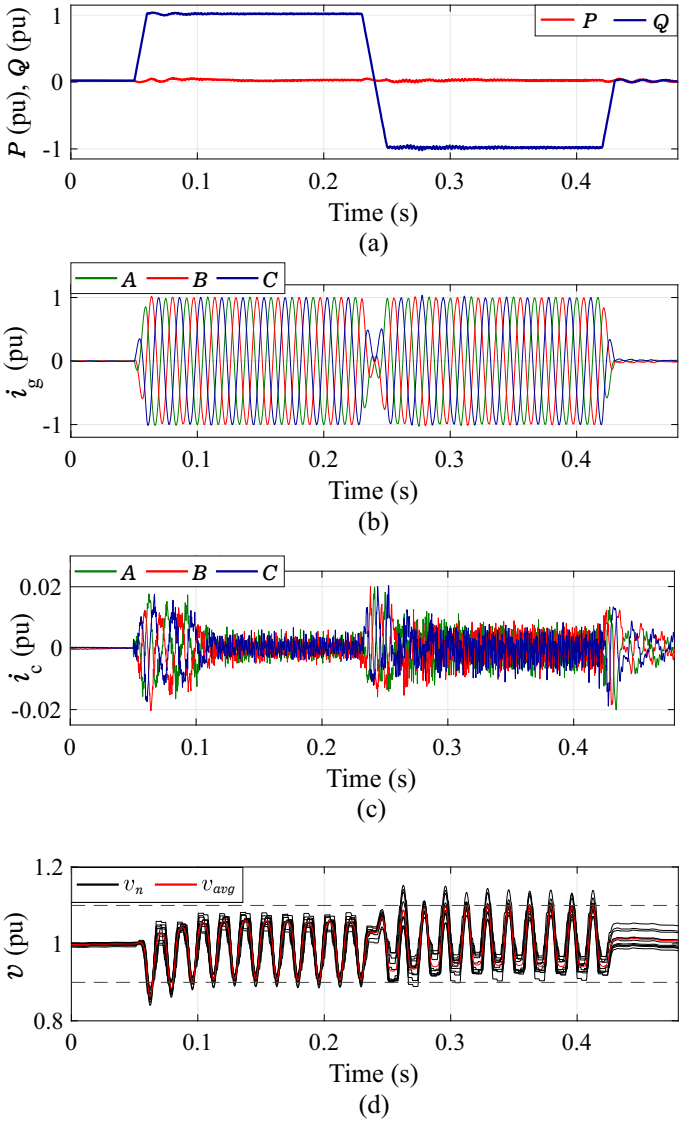
The SM capacitor voltages for the upper arm of phase A are presented in Fig. 27 (d). The gray dashed lines indicate the 10% tolerance band adopted in the capacitance design. As observed, during converter inductive operation, the capacitor voltage v_n waveforms present values smaller than the lower tolerance band. An analogous phenomenon is observed in the upper tolerance band during converter capacitive operation. Indeed, the energy storage requirements previously derived assume all capacitor voltages are perfectly balanced. Although there is a spread in the SM capacitors voltages, the average value of capacitor voltages v_{avg} is within the limits of the tolerance band validating the SM capacitor design.

2.3.1.4 PSI- and NSI-LVRT

Positive and negative sequence currents injection are considered in this case study aiming to fulfill both PSI- and NSI-LVRT accordingly to Fig. 12. The MSI strategy presented in (2.24)-(2.27) allows adjustment of the values of the k_+ and k_- parameters to set the ratio between the positive and negative sequence currents for given value of reactive power delivered to the grid.

An unbalanced grid voltage of $V^+ = 0.75$ and $V^- = 0.25$ is considered, as a consequence of a phase-to-ground fault occurring in the power system. In that way, the following operational conditions are analyzed:

Figure 27 – Dynamic behavior of HB-MMC in both inductive and capacitive reactive power operations: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents; (d) SM capacitor voltages.



Source: Elaborated by the author.

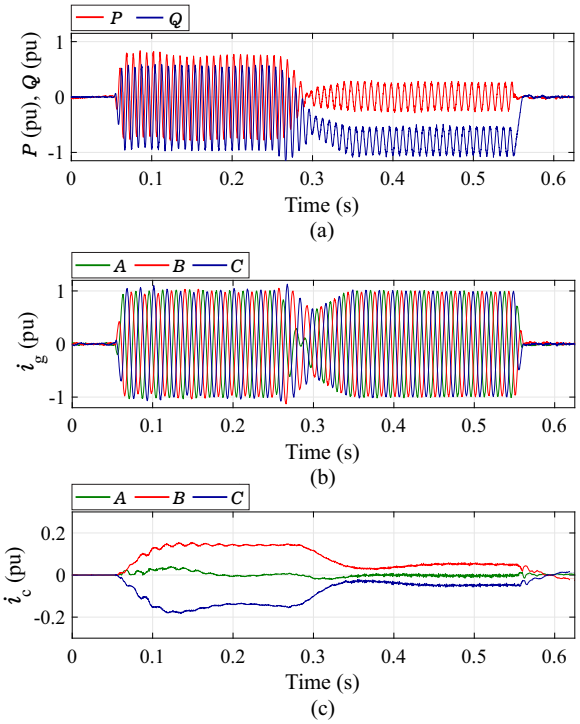
- $0.025s < t \leq 0.55s$: the fault is occurring and unbalanced grid voltages are presented;
- $0.05s < t \leq 0.25s$: only NSI-LVRT is adopted, considering $k_- = 10$ and $k_+ = 0$ for reducing the unbalance in the grid voltage;
- $0.25s < t \leq 0.35s$: MSI-LVRT is adopted. $k_- = 10$ is reduced to $k_- = 0$ with a slope of $-20/s$. Moreover, $k_+ = 0$ is increased to $k_+ = 10$ with a slope of $10/s$. Both changes are starting at $t = 0.25s$;
- $0.35s < t \leq 0.55s$: only PSI-LVRT is adopted, considering $k_- = 0$ and $k_+ = 10$ for supporting the grid voltage recovery;

The instantaneous active and reactive powers are presented in Fig. 28 (a). As observed, the instantaneous active and reactive power present oscillatory components at the doubled line frequency (120 Hz) during both PSI or NSI. Moreover, the amplitude of the oscillations in active and reactive power reaches around -1 pu, when 1 pu of inductive negative sequence reactive current is injected into the grid.

The grid currents are shown in Fig. 28 (b). As observed, the currents are unbalanced and the stresses in the converter phases are different when both sequences are processed during MSI. Even if the STATCOM injects around 1 pu of inductive negative sequence reactive current, the currents are not balanced, since there is an amount of absorbed positive sequence due to the MMC power losses. The circulating currents are presented in Fig. 28 (c). As noted, the circulating currents of phases B and C present a dc value when both PSI or NSI are considered. Furthermore, the circulating current of the phase B reached around 0.18 pu when the STATCOM injects 1 pu of inductive negative sequence reactive current. Indeed, the circulating currents present dc value during unbalanced conditions, as described in (2.37).

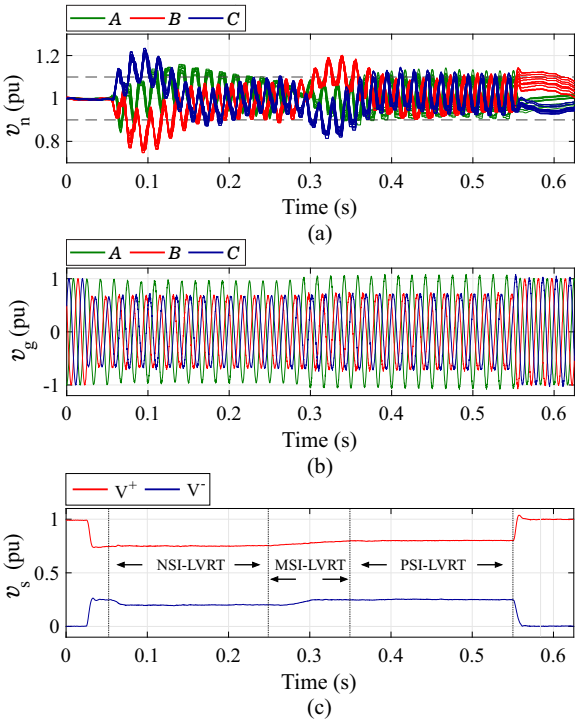
The SM capacitor voltages for the upper arms are presented in Fig. 29 (a). The

Figure 28 – Dynamic behavior of HB-MMC during LVRT: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents.



Source: Elaborated by the author.

Figure 29 – Dynamic behavior of HB-MMC during LVRT: (a) SM capacitor voltages; (b) Grid voltage; (c) Positive and negative *dq* grid voltage components.



Source: Elaborated by the author.

gray dashed lines indicate the 10% tolerance band adopted in the capacitance design. As observed, the SM capacitor voltage ripple depends on the values of positive and negative sequence currents. Different ripples are observed in each phase due the unbalanced currents. It is important to remark that the lower arms have similar behaviors to the respective upper arms. The maximum ripple in steady-state is around the 10% range adopted, even for the most stressed phases. During the transients, an overvoltage of around 20% can be observed, which are within the acceptance margins.

Figures 29 (b) and (c) present the grid voltages in natural coordinates *abc* and the positive and negative sequence voltages, respectively. As noted, only positive sequence voltage can be observed during the pre-fault condition. After the fault is detected in $t = 0.5s$, a decrease in V^- from 0.25 to 0.20 is achieved during NSI-LVRT, which indicates a reduction in the unbalanced grid voltage. In addition, V^+ is increased from 0.75 to 0.80, when only PSI-LVRT is enabled, which means support for grid voltage recovery. MSI-LVRT strategy can be used to provide both PSI and NSI by changing k_+ and k_-. However, the benefits of this strategy are limited to the range of both PSI and NSI strategies, since current limits of 1 pu for any of the converter phases are respected in this work.

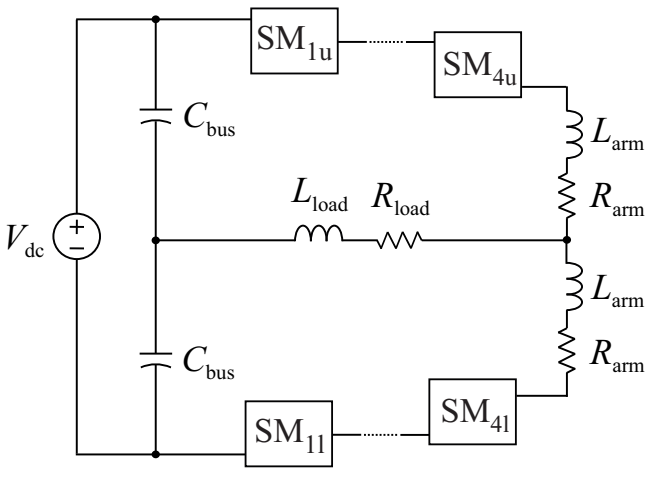
2.3.2 Experimental Results

To verify the validity of both theoretical and simulation analyses, experimental results were obtained for a low-voltage MMC prototype presented in Camurça et al. (2019). The results are obtained considering only a single-phase of the MMC connected to an RL load in an inverter operation, as shown in the circuit schematic in Fig. 30. The utilized MMC prototype was previously designed, in the way that the control strategies are the focus for implementation and validation. The main parameters are described in Table 7. As observed in Fig. 31 (a), the converter contains 4 FB-SMs (see Fig. 31 (b)) per arm

Table 7 – MMC main parameters for experimental results.

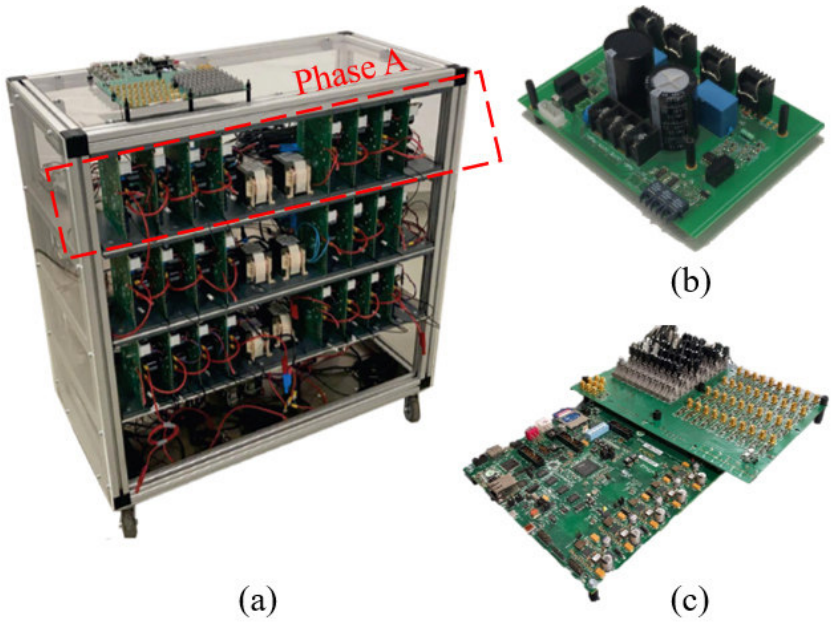
Parameter	Value
V_{dc}	400 V
P_{nom}	5 kW
N	4
V^*	100 V
C, C_{bus}	2 mF
L_{arm}, L_{load}	1.8 mH
R_{load}	100 Ω
f_c	5 kHz

Figure 30 – Schematic of the downscaled MMC prototype.



Source: Elaborated by the author.

Figure 31 – Downscaled MMC prototype (a) MMC; (b) FB-SM; (c) central control board (Zynq SoC ZC702).



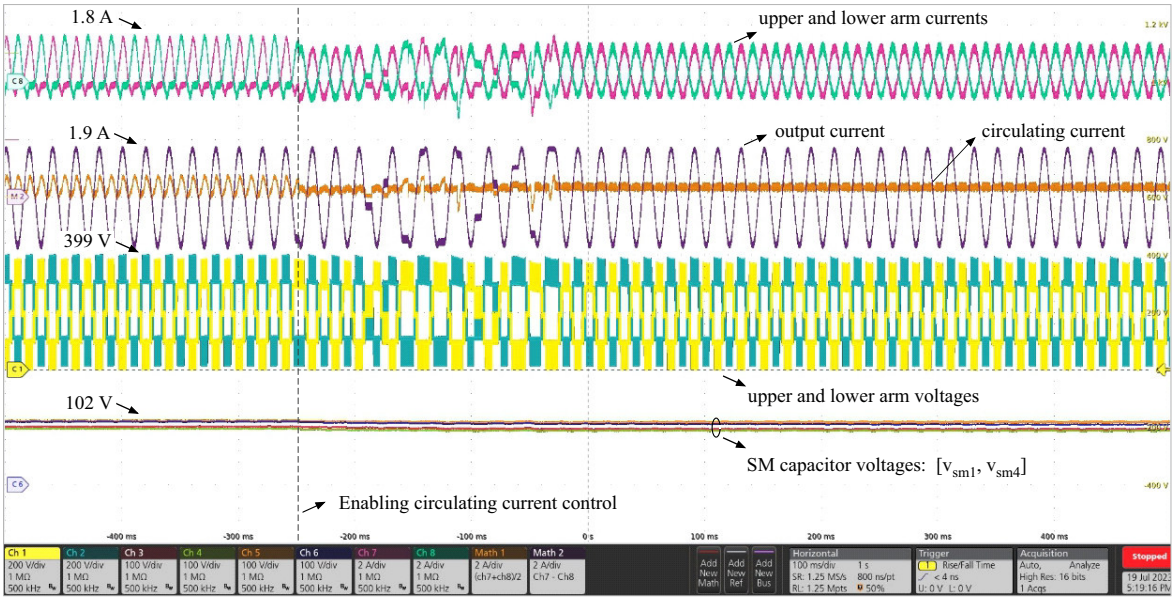
Source: Adapted from Camurça et al. (2019).

equipped with IGBTs, where only one bridge (HB) is operating. Also, the power stage presents isolated voltage measurements, semiconductor's driving circuitry and optical link connections for the command inputs of the central control board. The analog measurements from the isolated power stage are transmitted to the analog-to-digital converters (ADCs), which are in turn connected to the central controller. A central control board (Zynq SoC ZC702) is responsible for measurements conditioning, control loops and modulation, as shown in Fig. 31 (c).

Figure 32 presents the dynamic behavior for the single-phase MMC when enabling the circulating current control. In that case, the same strategy presented in the block diagram of 18 (b) is adopted. As observed, the 2nd harmonic component presented in both arm and circulating currents are almost completely suppressed after enabling the control. After around 200ms, the transient effect in the output current is extinguished and no effect of such control is observed in steady-state, as expected. A slightly deviation is observed in upper and lower arm voltages that can be explained by the effect of such control in the modulating signals obtained in (2.15). Such effects bring an SM capacitor voltage deviation which is hidden in a short time window (around 600ms), as presented in Fig. 32.

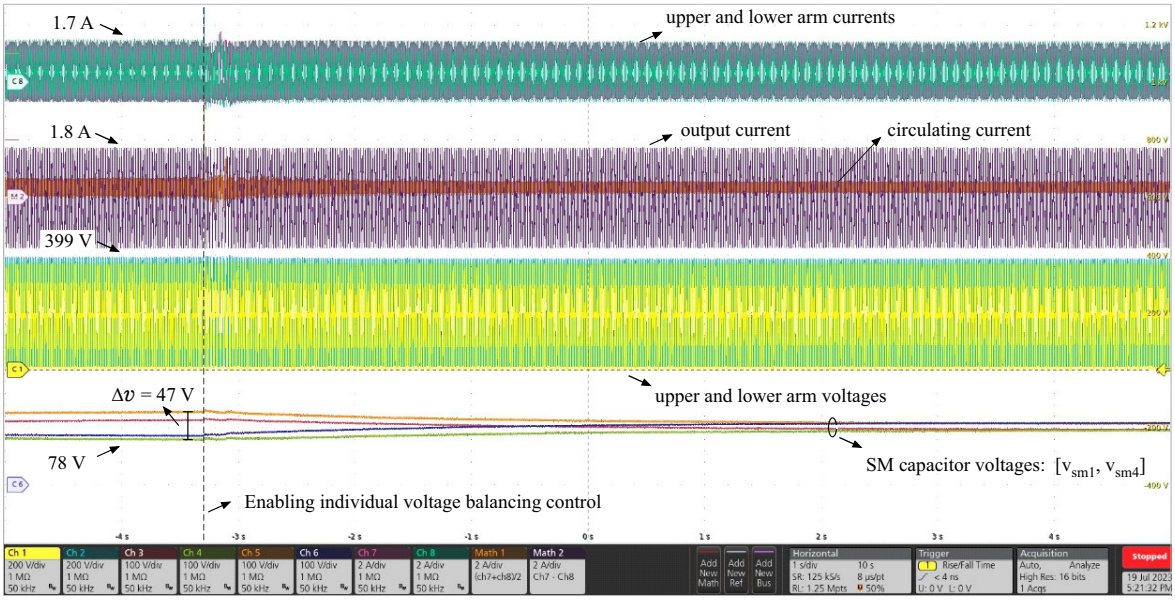
In that way, it is important to evaluate the individual voltage balancing control, as illustrated in Fig. 33. The same strategy presented in the block diagram of Fig. 18 (c) is adopted in this moment, with the exception of the moving average filter in the SM capacitor voltages. As noted, right before enabling such control technique, the relative standard

Figure 32 – Dynamic behavior of the single-phase MMC during the enabling of circulating current control.



Source: Elaborated by the author.

Figure 33 – Dynamic behavior of the single-phase MMC during the enabling of individual voltage balancing control.



Source: Elaborated by the author.

deviation among the SM capacitor voltage reached more than 20% and was slowing increasing, since an unstable operation is observed at this point due to the circulating current control. Enabling individual voltage balancing control could bring the SM capacitor voltages around the reference value $V^* = 100V$ in about 3s. Moreover, a transient effect on both arm and output currents is observed for about 300ms after enabling individual voltage balancing control.

2.4 Conclusions

In this chapter the topology, control and design of MMC-based STATCOM were presented. The dynamic response of the converter was analyzed for both PSI and NSI, meeting the LVRT requirements. Moreover, the converter energization was performed. The results showed satisfactory response of reactive power, grid current and circulating current, demonstrating effectiveness of the controls employed. Experimental results also validate the circulating current and capacitor voltage balancing controls.

The solutions based on the four semiconductor blocking voltages presented similar results in terms of dynamic performance, although hidden for simplicity. The main reason to define four different solutions is because the designs differ in terms of cost and reliability, which are evaluated in the next chapters.

3 A sliding-mode observer for MMC-based STATCOM systems

A sliding-mode observer for capacitor voltages estimation of the MMC-based STATCOM systems is adopted in this chapter, using the measurements of arm current and arm voltage. The observer performance is demonstrated through the same case studies employed in Chapter 2. A linear correction within the hysteresis band is included to reduce the chattering in observer dynamics. The effect of the switching and sampling frequencies on the observer performance is also evaluated.

3.1 Contextualization

The high number of SMs increases the number of electronic components in MMC, such as semiconductor switches and capacitors. In addition, the conventional control techniques employed in this converter are based on a high number of sensors and communication cables associated to the capacitor voltage measurements (Debnath et al., 2015). Therefore, some concerns regarding reliability have arisen and several MMC fault-tolerance methods have been proposed in recent years (Kadandani; Maiwada, 2015).

Some works present solutions based on SM capacitor voltage estimation for both the fault detection or the post-fault operation. Regarding the fault detection, these methods check the consistency between the actual system behavior and its observed behavior. Furthermore, the post-fault operation can be achieved via conceiving observer-based control strategies (Nademi; Das; Norum, 2015). Most observer-based control schemes rely on the capacitor current measurement, the knowledge of the converter parameters or their adaptive estimation (Nademi; Das; Norum, 2015; Picas et al., 2016). Other schemes use sliding-mode approaches to deal with parameter uncertainties (da Silva; Vieira; Rech, 2018). The main advantage in using methods based on capacitor voltage estimates is to reduce the burden of the data acquisition and the hardware complexity.

da Silva, Vieira and Rech (2018) propose a discrete sliding-mode observer to avoid sending all capacitor voltage measurements to the central processor, which reduces the requirements of the communication system. An arm-current sensorless capacitor-voltage-balancing method based on a state observer is proposed in (Hu; Teodorescu; Guerrero, 2019), which allows compacting the entire system and overall cost savings. Abushafa et al. (2018) propose an observer based on weighted recursive least square (RLS). The SM capacitor voltage estimation is performed through only one voltage measurement per MMC arm. A Kalman-filter-based estimation of SM voltages is presented in (Islam;

Razzaghi; Bahrani, 2020). The voltage measurement in the MMC arms is avoided by adding a correction factor to the previous observed capacitor voltages. Other observer method based on sample delay compensation is proposed in (Rong et al., 2018). This method replaces the measurements of each SM, measuring a set of SMs within the MMC arm. Abushafa et al. (2018) propose an integrated control strategy with fault detection and tolerance control capability. The capacitor voltage estimation is based on adaptive linear neuron (ADALINE) and RLS algorithms, which requires only three sensors per MMC phase, one for the phase voltage and two for the arm inductor voltages (Abdelsalam; Marei; Tennakoon, 2017).

Therefore, this work employs a sliding-mode observer using the measurements of arm current and arm voltage. A previous study about the adopted sliding-mode observer has been presented by Farias et al. (2023), with experimental validation of the method. In this sense, this observer is now evaluated for MMC-based STATCOM systems. Furthermore, the following contributions of this work can be highlighted in Table 8 comparing to the previous work in literature. The effect of switching and sampling frequencies on the observer are evaluated for only two frequency values in (da Silva; Vieira; Rech, 2018). In this sense, a range of typical switching frequencies applied to MMC is evaluated, proving that the increased spreading effect at low-switching frequencies is not caused by the adopted observer. Moreover, a decrease in chattering in the observed capacitor voltage is reached due the linear corrector.

Table 8 – Comparison of different capacitor voltage estimation methods.

Descriptions	**Silva et al.,** 2018	**Hu et al.,** 2019	**Abushafa et al.,** 2018	**Islam et al.,** 2020	**Rong et al.,** 2018	**Abdelsalam et al.,** 2017	**This work**
Reduced number of voltage measurement and data acquisition burden	+	+	+	++	-	++	+
Observability and stability proofs	Yes	Yes	No	Yes	Yes	Yes	Yes
Robustness to parameter uncertainties	++	++	++	++	++	+	++
Evaluation of the effect of switching and sampling frequencies on the observer	+	-	-	-	-	-	++
Gate signal required for the observer	No	Yes	Yes	Yes	Yes	Yes	Yes
Reduction of chattering in observer dynamics	No	No	No	No	No	No	Yes

++, + and - represent a good, moderate and low performance, respectively.

3.2 HB-MMC Switched Model

The MMC switched dynamics (quantities identified by the superscript s) of a generic MMC arm can be described by (Farias et al., 2023):

$$\overbrace{\begin{bmatrix} \dot{v}_1^s \\ \vdots \\ \dot{v}_N^s \\ \dot{i}_{arm}^s \end{bmatrix}}^{\dot{\boldsymbol{x}}} = \overbrace{\begin{bmatrix} 0 & \cdots & 0 & \frac{q_1}{C} \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & 0 & \frac{q_N}{C} \\ \frac{-q_1}{L_{arm}} & \cdots & \frac{-q_N}{L_{arm}} & \frac{-R_{arm}}{L_{arm}} \end{bmatrix}}^{A_{nl}(q)} \begin{bmatrix} v_1^s \\ \vdots \\ v_N^s \\ i_{arm}^s \end{bmatrix} + \begin{bmatrix} 0 \\ \vdots \\ 0 \\ \frac{0.5v_{dc}^s - v_{ac}^s}{L_{arm}} \end{bmatrix}, \tag{3.1}$$

where v_n^s are the instantaneous voltages of the SM capacitors and q_n are the gate signals applied to the SM upper-switch S_2 for $n = 1, \cdots, N$. Moreover, i_{arm}^s are the instantaneous arm currents of the upper or lower arms, v_{dc}^s are the instantaneous pole-to-pole dc voltages and v_{ac}^s is the instantaneous ac grid voltage. Under balanced conditions, the instantaneous per-pole dc voltage can be described by $0.5v_{dc}^s$. For the sake of simplicity, the subscripts u and l are omitted, since the equations for the upper or lower arms are equivalent.

The gate signals q_n determine the SM states, as well as the insertion of the SM capacitors into the MMC arm. Moreover, during the switching period T_c, $q_n = 1$ for $t \leq kT_c + t_{k-on}^n$ and $q_n = 0$ for $t_{k-on}^n < t \leq (k+1)T_c$, where t_{k-on}^n is the k-th switching time for the n-th SM, with $k = 0, 1, \cdots, \mathcal{N}$, the index number of the switching period in an $\mathcal{N}$ switching event series.

Furthermore, the system outputs can be described by:

$$\overbrace{\begin{bmatrix} v_{arm}^s \\ i_{arm}^s \end{bmatrix}}^{\boldsymbol{y}} = \overbrace{\begin{bmatrix} q_1 & \cdots & q_N & 0 \\ 0 & \cdots & 0 & 1 \end{bmatrix}}^{C_{nl}(q)} \begin{bmatrix} v_1^s \\ \vdots \\ v_N^s \\ i_{arm}^s \end{bmatrix}, \tag{3.2}$$

where v_{arm}^s are the sum of the instantaneous SM capacitor voltages of the upper or lower arms, which are inserted to the circuit. Therefore, the dynamics of the MMC output variables v_{arm}^s and i_{arm}^s are described by (3.1) and (3.2). Indeed, these are the input variables of the state observer adopted in this work.

3.3 SM Capacitor Voltage Observer

A capacitor voltage observer is adopted based on the HB-MMC switched model described above. Furthermore, aiming at robustness with respect to parameter uncertainty, the observed voltage value can be adjusted using a sliding-mode corrector. The capacitor voltage observer is given by:

$$\dot{\hat{v}}_n = \begin{cases} \overbrace{\frac{i_{arm}\, q_n}{C_{nom}}}^{\text{Estimate}} + \overbrace{\lambda\, q_n\, \text{sign}\,(e)}^{\text{Sliding-mode corrector}} & \text{if } |e| \geq V_{th}, \\ \overbrace{\frac{i_{arm}\, q_n}{C_{nom}}}^{\text{Estimate}} + \overbrace{\frac{\lambda}{V_{th}}\, q_n\, e}^{\text{linear corrector}} & \text{if } |e| < V_{th}, \end{cases} \tag{3.3}$$

$$\text{for } \; e = \sum_{n=1}^{N} q_n v_n - \sum_{n=1}^{N} q_n \hat{v}_n = v_{arm} - \hat{v}_{arm}, \tag{3.4}$$

where λ is the observer correction gain, C_{nom} is the nominal SM capacitance and V_{th} is the hysteresis band voltage. The arm voltage measurement v_{arm} and the arm current measurement i_{arm} are the observer inputs. As noted, within a hysteresis band ($-V_{th} < e < V_{th}$), the sliding-mode observer is a standard proportional type. Indeed, when this error tends to zero, a reduction in the correction effect is expected avoiding chattering in observer dynamics. The introduction of the proportional correction in the hysteresis band is evaluated in Section 3.7 of this work.

Furthermore, the function sign in (3.3) returns either -1, 0, or 1, according to the error signal. As noted, sign function is multiplied not only by λ but also by the SM upper-switch gate signals q_n, thus ensuring that the correction is only applied to the SMs used to calculate the error. Under such conditions, the adopted observer presents fast convergence, as well as interesting dynamic features.

As noted, the adopted observer in (3.3) needs a gate signal applied to the SM, i.e., the converter must be in CM. However, during the energization of the converter, there is no pulse applied to either the upper or lower switches of the SM. Therefore, to obtain the right behavior of the adopted observer during NRM, q_n must be modified by the following switching function:

$$q_n = \begin{cases} 1, & \text{if } i_{arm} > 0, \\ 0, & \text{if } i_{arm} \leq 0. \end{cases} \tag{3.5}$$

In the next sections, the stability and robustness proofs of the observer are evaluated, as well as the system observability.

3.4 Stability and Robustness Proofs

The observed SM capacitor voltages are given in (3.3) as a summation of integrals in each switching interval T_c, which is derived from the HB-MMC switched model. However, the dynamic of the HB-MMC switched model tends, in average, to an averaged non-linear

model. Thus, the stability and robustness proofs of the observer is based on the HB-MMC averaged non-linear model described below.

3.4.1 Averaged Non-linear Model

A non-linear state-space model of the averaged system is derived as follows:

$$\begin{bmatrix} \dot{v}_1 \\ \vdots \\ \dot{v}_N \\ \dot{i}_{arm} \end{bmatrix} = \overbrace{\begin{bmatrix} 0 & \cdots & 0 & \frac{g_1}{C} \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & 0 & \frac{g_N}{C} \\ \frac{-g_1}{L_{arm}} & \cdots & \frac{-g_N}{L_{arm}} & \frac{-R_{arm}}{L_{arm}} \end{bmatrix}}^{A_{nl}(g)} \begin{bmatrix} v_1 \\ \vdots \\ v_N \\ i_{arm} \end{bmatrix} + \begin{bmatrix} 0 \\ \vdots \\ 0 \\ \frac{0.5v_{dc}-v_{ac}}{L_{arm}} \end{bmatrix}, \tag{3.6}$$

where g_n are the SM duty cycles of the upper or lower arm for $n = 1, \cdots, N$, i.e., $g_n = \frac{1}{T_c}\int_{t-T_c}^{t} q_n(\tau)d\tau$, which provides the fraction of the switching period when the capacitor is inserted into the MMC arm. The quantities v_n, i_{arm}, v_{arm}, v_{dc} and v_{ac} are the average values in the switching interval, defined as: $v_n = \int_{t-T_c}^{t} v_n^s(\tau)d\tau$, $i_{arm} = \int_{t-T_c}^{t} i_{arm}^s(\tau)d\tau$, $v_{arm} = \int_{t-T_c}^{t} v_{arm}^s(\tau)d\tau$, $v_{dc} = \int_{t-T_c}^{t} v_{dc}^s(\tau)d\tau$ and $v_{ac} = \int_{t-T_c}^{t} v_{ac}^s(\tau)d\tau$, respectively.

Therefore, the average MMC output variables are given by:

$$\overbrace{\begin{bmatrix} v_{arm} \\ i_{arm} \end{bmatrix}}^{\boldsymbol{y}} = \overbrace{\begin{bmatrix} g_1 & \cdots & g_N & 0 \\ 0 & \cdots & 0 & 1 \end{bmatrix}}^{C_{nl}(g)} \begin{bmatrix} v_1 \\ \vdots \\ v_N \\ i_{arm} \end{bmatrix}, \tag{3.7}$$

which describes a non-linear (bilinear) system, since matrices $A_{nl}(g)$ and $C_{nl}(g)$ in (3.6) and (3.7) are functions of the duty cycles g_n.

3.4.2 Stability Proof

The differential equations of the SM capacitor voltages can be obtained from (3.6) as:

$$\dot{v}_n = \frac{i_{arm}\, g_n}{C}, \tag{3.8}$$

where C is the actual value of the SM capacitance. Considering that $C = C_{nom}$, the observer error $\tilde{v}_n = v_n - \hat{v}_n$, is obtained by (3.8) and (3.3), as follows:

$$\dot{\tilde{v}}_n = \dot{v}_n - \dot{\hat{v}}_n = \begin{cases} -\lambda\, g_n \,\text{sign}\left(\sum_{n=1}^{N} g_n \tilde{v}_n\right), & \text{if } |e| \geq V_{th}, \\ \\ -\frac{\lambda}{V_{th}}\, g_n \, \sum_{n=1}^{N} g_n \tilde{v}_n. & \text{if } |e| < V_{th}. \end{cases} \tag{3.9}$$

Let,

$$\begin{gathered} \boldsymbol{v} = [v_1, \cdots, v_N]^T, \qquad \hat{\boldsymbol{v}} = [\hat{v}_1, \cdots, \hat{v}_N]^T, \\ \boldsymbol{s} = \boldsymbol{v} - \hat{\boldsymbol{v}} = \tilde{\boldsymbol{v}} = [\tilde{v}_1, \cdots, \tilde{v}_N]^T, \end{gathered} \tag{3.10}$$

be an N dimension vector defining a surface $s = 0$. Moreover, the Lyapunov function candidate is described by:

$$V_{lf} = \frac{1}{2}\boldsymbol{s}^T\boldsymbol{s}. \tag{3.11}$$

Therefore, the time derivative of V_{lf} is:

$$\dot{V}_{lf} \;=\; \boldsymbol{s}^T\dot{\boldsymbol{s}} = \begin{cases} -\lambda \left|\sum_{n=1}^{N} g_n \tilde{v}_n\right| \leq 0, & \text{if } |e| \geq V_{th}, \\ \\ -\frac{\lambda}{V_{th}} \sum_{n=1}^{N} g_n \tilde{v}_n^2 \leq 0, & \text{if } |e| < V_{th}. \end{cases} \tag{3.12}$$

Thus, equation (3.12) guarantees stability and asymptotic convergence of the observer for any $\lambda > 0$.

3.4.3 Robustness

The observed voltages based on sliding-mode observers present robustness to parameter uncertainties (e.g., SM capacitance values). To evaluate the observer robustness, the differential equations of the observed SM capacitor voltages for the error outside the hysteresis band ($|e| \geq V_{th}$) can be obtained from (3.3) as:

$$\dot{\hat{v}}_n = \frac{i_{arm}\, g_n}{C_{nom}} + \lambda\, g_n \,\text{sign}\,(e)\,. \tag{3.13}$$

Under such conditions, the derivative of the Lyapunov function of (3.12) for the error outside the hysteresis band is given as:

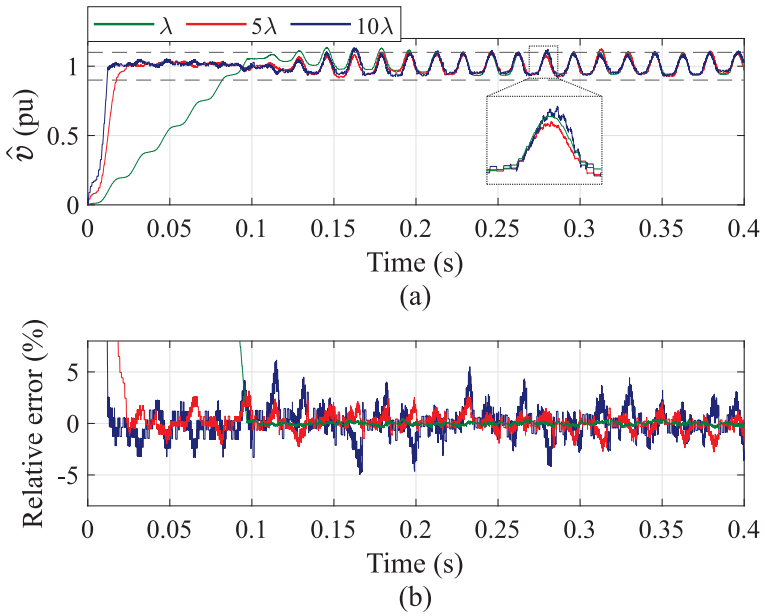
$$-\lambda \left|\sum_{n=1}^{N} g_n \tilde{v}_n\right| + \epsilon\, i_{arm} \sum_{n=1}^{N} g_n \tilde{v}_n \leq (-\lambda + |\epsilon\, \sigma|) \left|\sum_{n=1}^{N} g_n \tilde{v}_n\right| \leq 0, \tag{3.14}$$

where $\epsilon = \frac{1}{C} - \frac{1}{C_{nom}}$ is the worst-case discrepancy in C, and $\sigma > |i_{arm}|$ is an upper bound of MMC arm current i_{arm}. From (3.14), the error is confined within the hysteresis band for $\lambda > |\epsilon\,\sigma|$, which can be rewritten as:

$$\lambda > \lambda^* = \left| i_{arm} \left(\frac{1}{C} - \frac{1}{C_{nom}} \right) \right|. \tag{3.15}$$

In addition, the upper bound criteria for the observer gain can be determined by the effect caused by the discretized controller, since the observer correction is applied in the sampling time causing oscillation in the estimation. Figure 34 shows the observer performance for different observer gains, considering 1 pu of reactive power injected into the grid at $t = 100$ ms. For the sake of simplicity, only one SM capacitor voltage in the upper arm of MMC phase A is shown. As noted in Fig. 34 (a), the measured voltage reaches the reference in about 10 ms considering 10λ, where $\lambda = 46000$ is employed according to the MMC parameters in Tab. 5. Moreover, a small gain increases the required time for convergence. It is important to remark that for the observer gain equals λ, the steady-state is achieved in about 100 ms with low oscillation, as illustrated in detail in Fig. 34 (b). In Section 3.7, optimal λ is founded empirically through simulations.

Figure 34 – Evaluation of the observer performance for different λ: (a) Observed voltage; (b) Relative error. *Remark:* the switching frequency is $f_c = 1$ kHz and sampling frequency is $f_s = 22$ kHz.



Source: Elaborated by the author.

3.5 System Observability

The electrical dynamics of the MMC, given by (3.1), is both nonlinear and discontinuous due to the bilinear and switching characteristics of the system. Nevertheless, the average model dynamics of the MMC, given by (3.6), is smooth and can be considered to estimate the average unmeasured variables, such as SM capacitor voltages. This section considers two conditions for observability. Firstly, local stability for the linearized system, and secondly, an alternative and more general type of observability, known as $Z(T_{\mathcal{N}})$-Observability, proposed in (Kang; Barbot, 2007).

3.5.1 Linearized System Model

To establish the system local observability, a linearization is carried out around a certain operating point (X, U), and a small-signal linear model is derived, with $\boldsymbol{X} = [V_1, \cdots, V_N, I_{arm}]^T$, $\boldsymbol{U} = [\bar{g}_1, \cdots, \bar{g}_N, I_{arm}]^T$ and $\boldsymbol{Y} = [V_{arm}, I_{arm}]^T$. Let $\boldsymbol{x} = [v_1, \cdots, v_N, i_{arm}]^T$ be the state vector of the non-linear system, $\boldsymbol{u} = [g_1, \cdots, g_N, i_{arm}]^T$ the input vector, $\boldsymbol{y} = [v_{arm}, i_{arm}]^T$ the measured output. Furthermore, $\boldsymbol{x_s} = \boldsymbol{x} - \boldsymbol{X}$, $\boldsymbol{u_s} = \boldsymbol{u} - \boldsymbol{U}$ and $\boldsymbol{y_s} = \boldsymbol{y} - \boldsymbol{Y}$ are the small-signal state, input and output vectors, respectively, of the linearized system around an operation point given by constant duty cycles $\boldsymbol{U}$, a constant state vector $\boldsymbol{X}$, and a constant output $\boldsymbol{Y}$, such that:

$$\begin{aligned} \dot{\boldsymbol{x}}_{\boldsymbol{s}} &= \overbrace{\left.\frac{\partial F(x,u)}{\partial x}\right|_{\boldsymbol{X},\boldsymbol{U}}}^{A_l} \boldsymbol{x_s} + \overbrace{\left.\frac{\partial F(x,u)}{\partial u}\right|_{\boldsymbol{X},\boldsymbol{U}}}^{B_l} \boldsymbol{u_s}, \\ \boldsymbol{y_s} &= \overbrace{\left.\frac{\partial G(x,u)}{\partial x}\right|_{\boldsymbol{X},\boldsymbol{U}}}^{C_l} \boldsymbol{x_s} + \overbrace{\left.\frac{\partial G(x,u)}{\partial u}\right|_{\boldsymbol{X},\boldsymbol{U}}}^{D_l} \boldsymbol{u_s}, \end{aligned} \tag{3.16}$$

where $F(x,u) = A_{nl}(g)x$ and $G(x,u) = C_{nl}(g)x$. Moreover, considering $\boldsymbol{u_s} = [g_{s_1}, \cdots, g_{s_N}, i_{s_{arm}}]^T$, the linear matrices of the small-signal model in (3.16) are given by:

$$A_l = \begin{bmatrix} 0 & \cdots & 0 & \frac{\bar{g}_1}{C} \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & 0 & \frac{\bar{g}_N}{C} \\ \frac{-\bar{g}_1}{L_{arm}} & \cdots & \frac{-\bar{g}_N}{L_{arm}} & \frac{-R_{arm}}{L_{arm}} \end{bmatrix} B_l = \begin{bmatrix} \frac{I_{arm}}{C} & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & \frac{I_{arm}}{C} & 0 \\ \frac{-V_1}{L_{arm}} & \cdots & \frac{-V_N}{L_{arm}} & \frac{-1}{L_{arm}} \end{bmatrix}, \tag{3.17}$$

$$C_l = \begin{bmatrix} \bar{g}_1 & \cdots & \bar{g}_N & 0 \\ 0 & \cdots & 0 & 1 \end{bmatrix} D_l = \begin{bmatrix} V_1 & \cdots & V_N & 0 \\ 0 & \cdots & 0 & 0 \end{bmatrix}. \tag{3.18}$$

3.5.2 Linear System Observability

It can be seen that the state vector x is not globally observable, i.e., the rank r of the observability matrix is $r = 2 < N$:

$$O = \begin{bmatrix} C_l & C_l A_l & \cdots & C_l A_l^{N-1} \end{bmatrix}^T.$$

Nevertheless, the individual capacitor voltages v_n for $n = 1, \cdots, N$ are observable locally, considering the remaining capacitor voltages as perturbations. The resulting individual small-signal dynamics is given by (3.19) and (3.20).

$$\overbrace{\begin{bmatrix} \dot{v}_{s_n} \\ \dot{i}_{s_{arm}} \end{bmatrix}}^{\dot{\boldsymbol{x}}_{\boldsymbol{sn}}} = \overbrace{\begin{bmatrix} 0 & \frac{\bar{g}_n}{C} \\ \frac{-\bar{g}_n}{L_{arm}} & \frac{-R_{arm}}{L_{arm}} \end{bmatrix}}^{A_n} \begin{bmatrix} v_{s_n} \\ i_{s_{arm}} \end{bmatrix} + \overbrace{\begin{bmatrix} \frac{I_{arm}}{C} \\ \frac{-V_n}{L_{arm}} \end{bmatrix}}^{B_n} g_{s_n} - \begin{bmatrix} 0 \\ \frac{\varphi}{L_{arm}} \end{bmatrix}, \tag{3.19}$$

$$\overbrace{\begin{bmatrix} v_{s_{arm}} \\ i_{s_{arm}} \end{bmatrix}}^{\boldsymbol{y}} = \overbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}^{C_n} \begin{bmatrix} v_{s_n} \\ i_{s_{arm}} \end{bmatrix} + \begin{bmatrix} \varphi \\ 0 \end{bmatrix}. \tag{3.20}$$

It is important to remark that $v_{s_{arm}}$, $i_{s_{arm}}$, v_{s_n} and g_{s_n} are small signals of the arm voltage, the arm current, the n-th capacitor voltage and the n-th capacitor duty-cycle, respectively. The perturbation term φ is given as:

$$\varphi = \sum_{\substack{k=1 \\ k \neq n}}^{N} \bar{g}_k v_{s_k}, \tag{3.21}$$

Now, the observability matrix $O_n = [C_n, C_n A_n]^T$ has rank $r = 2$, which is the order of the subsystem. The capacitor voltage for each SM can be estimated using the arm current and its gate signals. Notice that $0 < g_n < 1$ corresponds to the duty cycle applied to the SM upper-switch (S_2) over the period T.

3.5.3 $Z(T_N)$-Observability

The Z-Observability is an observability concept introduced by (Kang; Barbot, 2007) for smooth systems, and the $Z(T_N)$-observability is a specific case applied for the following class of switched systems:

$$\begin{aligned} \dot{\boldsymbol{\xi}} &= \boldsymbol{f_q}(t, \xi, u), \ \boldsymbol{q} \in Q_f, \ \boldsymbol{\xi} \in \Re^n, \ \boldsymbol{u} \in \Re^m, \\ \boldsymbol{Y} &= \boldsymbol{h_q}(t, \xi, u), \end{aligned} \tag{3.22}$$

where Q_f is a finite index set, $\boldsymbol{f_q}\Re \times \Re^n \times \Re^m \to \Re^m$ sufficiently smooth, the dwell time $[t_{i,0}, t_{i,1}]$ between two switches (i.e., change of q) satisfies: $\exists \tau_{min} > 0$ such that

$(t_{i,1} - t_{i,0}) > \tau_{min}$. It is also assumed that the input $u(t)$ is bounded and C^{∞} at any time interval $[t_{i,0}, t_{i,1}[\subseteq [t_{ini}, t_{end}]$. This observability is conceived in terms of the switched system dynamics and a given hybrid time trajectory whose definition is given in (Kang; Barbot, 2007).

In this work, the system described in (3.22) has (3.1) for $\boldsymbol{f_q}(t, \xi, u)$ and (3.2) for $\boldsymbol{h_q}(t, \xi, u)$. Given the characteristics of the MMC operating with interleaved switching periods, for each switching period T_c there are at most $2N$ sets of $\boldsymbol{f_q}(t, \xi, u)$ and $\boldsymbol{h_q}(t, \xi, u)$, and the minimum dwell time condition between two switches, required by the $Z(T_{\mathcal{N}})$-observability definition, is always satisfied.

3.5.4 Observability Definitions

It follows from the $Z(T_{\mathcal{N}})$-observability that a hybrid trajectory of voltage outputs $v_{arm}(t, \boldsymbol{x}, \boldsymbol{q})$ and switching functions $\boldsymbol{q}$, i.e., a sequence of $\boldsymbol{q}$ such that N of them are linearly independent, guarantees the observability of the capacitor voltages. Moreover, the information in a sequence of outputs allows to retrieve the individual capacitor voltages. Therefore, unlike the local definition of observability of the capacitor voltages for the resulting averaged linearized system, the $Z(T_{\mathcal{N}})$-observability is rather broad and comprehensive for non-linear switched systems.

3.6 Discussion

The SM capacitor voltage control is performed by the knowledge of each SM capacitor voltage in real-time, typically requiring a SM capacitor voltage measurement for each SM to be transmitted to the controller. In this sense, following the centralized control architecture from Fig. 22 (a), the number of measured signals received by the main controller in the HB-MMC can be described by:

$$N_{signals} = 6N + 9, \tag{3.23}$$

where 6 arm current measurements and 3 grid voltage measurements are considered per HB-MMC. By implementing the presented sliding-mode observer, no SM capacitor voltage measurement is needed to be transmitted to the main controller. In such case, one additional voltage measurement is required per MMC arm (sometimes also required in the previous configuration). Therefore, (3.23) can be rewritten as:

$$N_{signals} = 15. \tag{3.24}$$

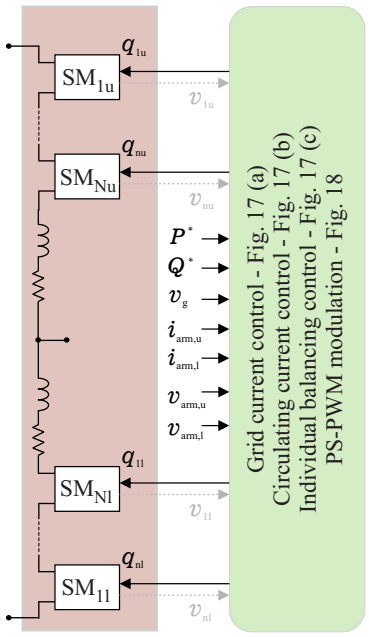
From (3.23) and (3.24), a reduction of the number of measured signals received by the main controller is achieved for $N > 1$. For the sake of simplicity, only the main changes

on the control architecture in comparison to Fig. 22 (a) for one MMC phase are highlighted in Fig. 35, when adopting the presented sliding-mode observer. Similar behavior can be reached by using decentralized control architecture, where the signals $v_{n,ul}$ in Fig. 22 (b) can be also disregarded. It is important to remark that the proposed method with only one arm voltage measurement is much more impaired by a sensor failure. This issue can be solved with redundant arm voltage measurement, which is a common practice in some industry segments.

For the proper operation of the observer, the measured arm voltages and the gate signals must be synchronized. Since, the moment when gate signals are produced is known, as well as the latency introduced by the measurement, the driving signals can be delayed to match the measured voltage. Moreover, the voltage balancing algorithm presents slow time constants if compared with the current control. In that sense, adding latency to the measurement has little effect to the MMC control.

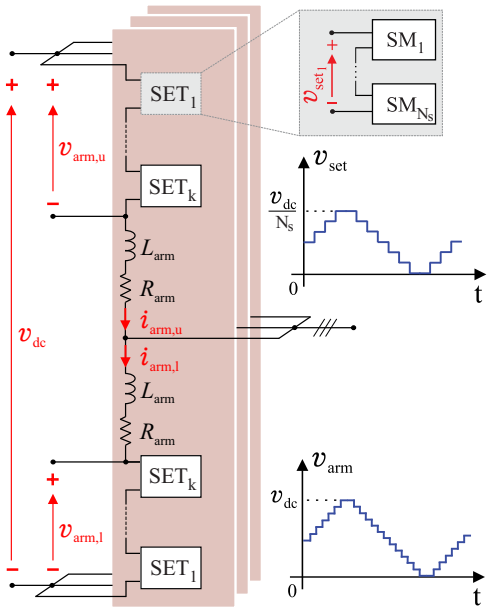
Another important point is the accuracy required for the arm voltage sensor. In some MMC applications, the voltage of a single SM is lower than 1% of the whole arm voltage. In this case, sensor accuracy can affect the performance of the adopted observer. This issue can be avoided by measuring a set of SMs (Rong et al., 2018), as shown in Fig. 36. As noted, the SMs are divided into k sets with N_s SMs, where each set only needs one

Figure 35 – Conceptual centralized MMC control architecture considering SM capacitor voltage observers. *Remark:* only one MMC phase is illustrated.



Source: Adapted from Sharifabadi et al. (2016).

Figure 36 – Schematic of a three-phase MMC with sets of SMs.



Source: Elaborated by the author.

voltage sensor. In this case, the adopted observer is employed for each set of SMs, and a partial reduction in the MMC hardware complexity is reached.

3.7 Results

This section aims to validate the sliding-mode observer in terms of dynamic and steady-state performances of the HB-MMC, operating during both positive and negative sequences injection. All simulations were performed in PLECS environment based on the topology presented in Fig. 15. The same case studies presented in Section 2.3 are investigated for the sliding-mode observer operation. The observer is employed and the SM capacitor voltages are measured only to validate the performance. The observer gain $\lambda = 46000$ are chosen, respecting the limits defined in Section 3.4.3. In addition, $V_{th} = 0.02V^*$ is employed.

The presented results are based only on the C_{45} solution, which employs semiconductor block voltage of 4.5 kV. Moreover, all results are presented in pu in the base values illustrated in Tab. 5.

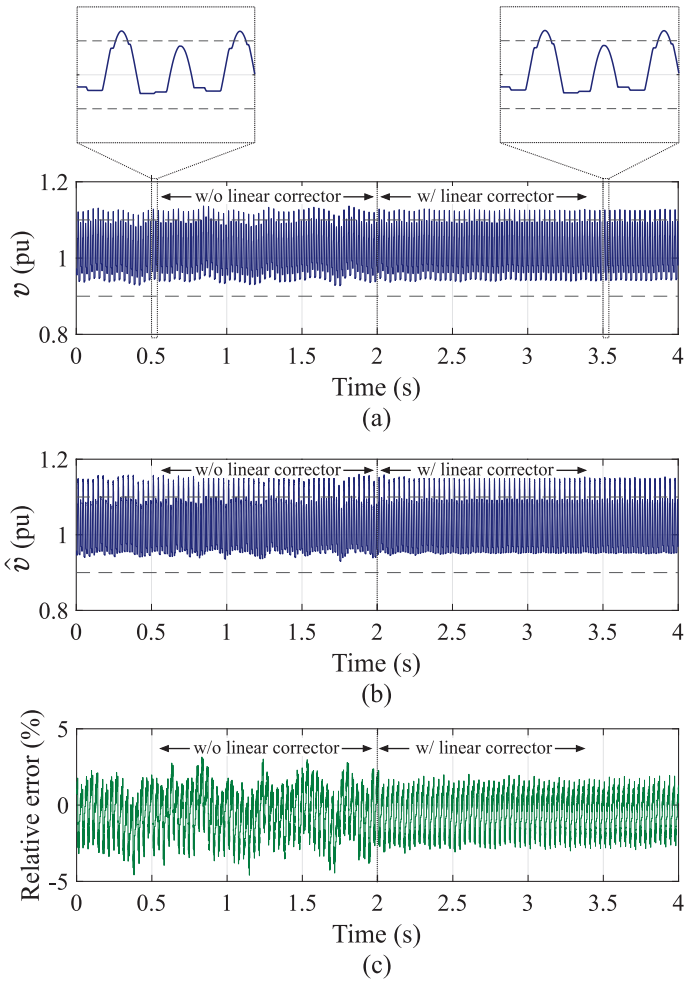
3.7.1 Linear corrector evaluation

For the sake of simplicity, only one SM in the upper arm of MMC phase A is analyzed. Aiming to evaluate the observer to uncertainty parameters, the value of the SM capacitances is inserted into the model considering a tolerance of 10% with normal distribution. Initially, the observer is operating without the proposed linear corrector. After $t = 2s$, the linear corrector is added. As noted in detail in Fig. 37 (a), the v_1 waveform is very similar for both operations. However, the effect caused by the linear corrector results in a decrease in low-frequency chattering in the observed capacitor voltage $\hat{v}_1$, which leads to smoother waveforms in both v_1 and $\hat{v}_1$, as shown in Figs. 37 (a) and (b), respectively. Furthermore, this effect can be also noted in relative error between the measured and estimated value in Fig. 37 (c). The relative error reaches values around $\pm$ 4.2% without the linear corrector, while values within $\pm$ 2.7% are obtained, when the linear corrector is considered.

3.7.2 Steady-State Performance

In steady-state operation, 1 pu of reactive power injected into the grid is considered. Figure 38 (a) shows the effect of both the SM capacitance tolerance and the switching frequency in the maximum relative error. As noted, a reduced capacitance tolerance value reduces the maximum relative error. Moreover, an increased switching frequency tends to reduce the maximum relative error. The measured and observed SM capacitor voltage

Figure 37 – Evaluation of the observer performance with and without linear corrector: (a) Measured voltage; (b) Observed voltage; (c) Relative error.



Source: Elaborated by the author.

waveforms are illustrated in detail in the next sections, considering $f_{sw} = 210$ Hz and an SM capacitance tolerance of 10% with normal distribution.

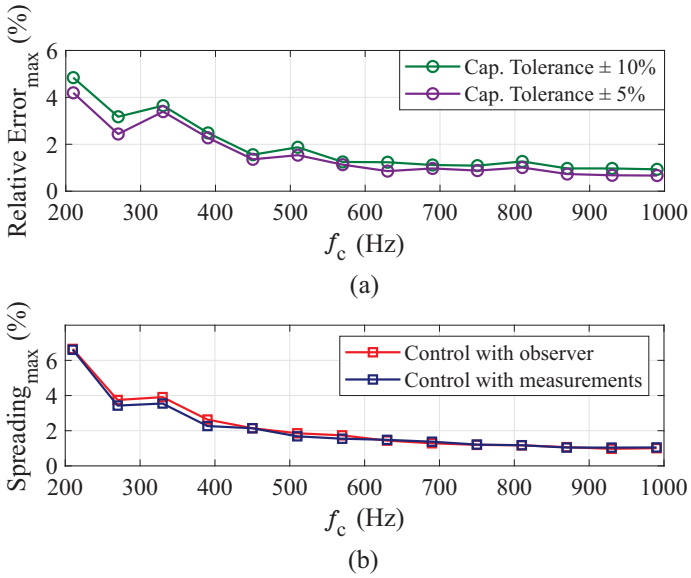
Figure 38 (b) shows the effect of the adopted observer on the spreading of the SM capacitor voltages [1]. As noted, the spreading of capacitor voltages is similar in both strategies. Therefore, the increased spreading effect at low-switching frequencies is not caused by the adopted observer. Indeed, the spreading in capacitor voltages at low-switching frequencies is an expected effect in MMC.

3.7.3 HB-MMC energization

The charging resistors limit the in-rush current during the pre-charge operation in NRM until the converter operates in CM. The pre-charge time intervals are defined as in Section 2.3.1.2.

[1] It is important to remark that only in this case, the MMC control is carried out in both situations: with voltage measurements and with observed voltages

Figure 38 – Steady-state performance at 1 pu of reactive power injected into the grid. (a) Effect of capacitance tolerance and switching frequency on the maximum relative error among all SM voltage measurements and estimates; (b) Maximum spreading of the capacitor voltages. *Remark:* the sampling frequency is $f_s = 2Nf_c$. $\lambda_{5\%} = 22000$ and $\lambda_{10\%} = 46000$.

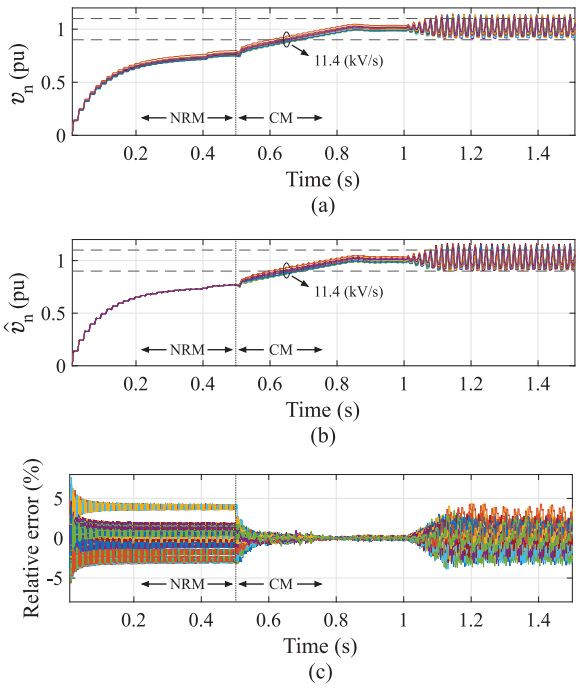


Source: Elaborated by the author.

Measured and observed SM capacitor voltages are illustrated in Figs. 39 (a) and (b), respectively. The dashed lines indicate that the SM capacitor voltages oscillate with 10% of ripple. Furthermore, the value of the SM capacitances is inserted into the model considering a tolerance of 10% with normal distribution. As observed, the SM capacitors are charged up to $\frac{\widehat{V}_g}{N}$, which is the limit value reaches in NRM by the ac-side pre-charge. Under such conditions, the relative errors between the measured and estimated values are within ± 5%, as shown in Fig. 39 (c). During CM, the SM capacitors are charged up to V^* in ramp with slope 11.4 kV/s, and the relative errors are also within ± 5%.

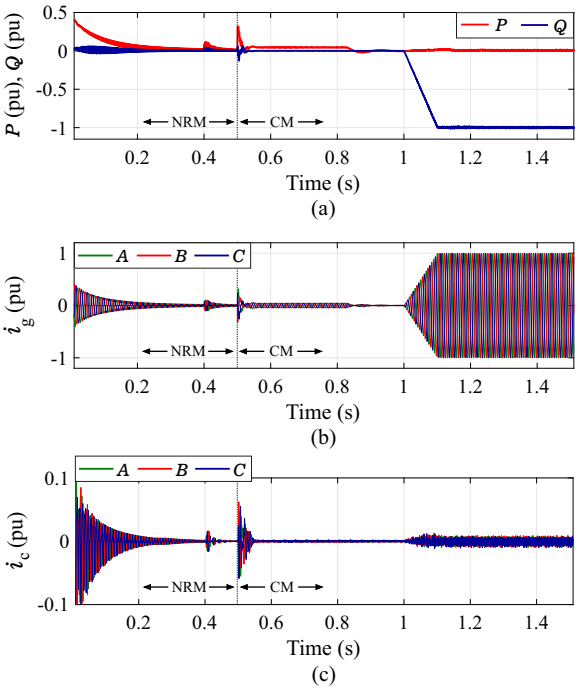
Figure 40 (a) shows the reactive and active power flows. Initially, the closed-loop control is disabled. The active power is absorbed from the grid during NRM, since the SM capacitors must be charged. After t = 1s, the converter is brought to the nominal operating condition reaching -1 pu of reactive power in capacitive operation. Moreover, the active power presents an average value less than 0.01 pu, which corresponds to the MMC power losses. The grid and circulating currents are illustrated in Figs. 40 (b) and (c), respectively. As observed, the grid current is limited in NRM. When the reactive power reference in ramp with slope of -1700 Mvar/s is employed, the grid current amplitude increases. Regarding the circulating currents, no dc value is presented, since only reactive power is processed by the converter. In the nominal operating condition, the circulating currents presented a ripple around 0.01 pu, against 0.007 pu, when the measured capacitor voltages are utilized in the control.

Figure 39 – SM capacitor voltages of the upper arm of MMC phase A during energization condition: (a) Measured voltages; (b) Observed voltages; (c) Relative errors.



Source: Elaborated by the author.

Figure 40 – Dynamic behavior of HB-MMC during energization condition: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents.



Source: Elaborated by the author.

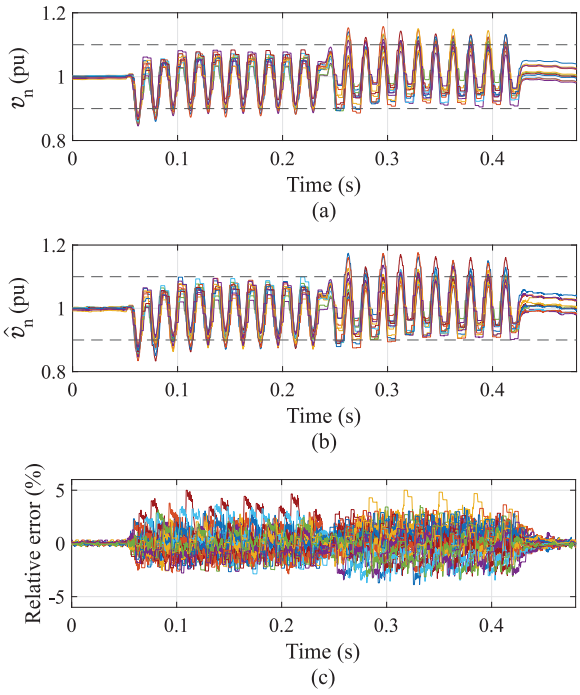
3.7.4 Positive Sequence Injection

In this case study, only positive sequence injection is considered. Under such conditions, the trapezoidal reactive power profile presented in Fig. 26 is employed.

Measured and observed SM capacitor voltages are illustrated in Figs. 41 (a) and (b), respectively. The gray dashed lines indicate the 10% tolerance band adopted in the capacitance design. As noted, the values defined by the tolerance band are slightly exceeded during both operations. It is important to note that this condition also occurs when the measured capacitor voltages are utilized in the control, since the energy storage requirements previously derived assume all capacitor voltages are perfectly balanced. Moreover, the relative errors between the measured and estimated values are within $\pm$ 5% for both operations, as shown in Fig. 41 (c).

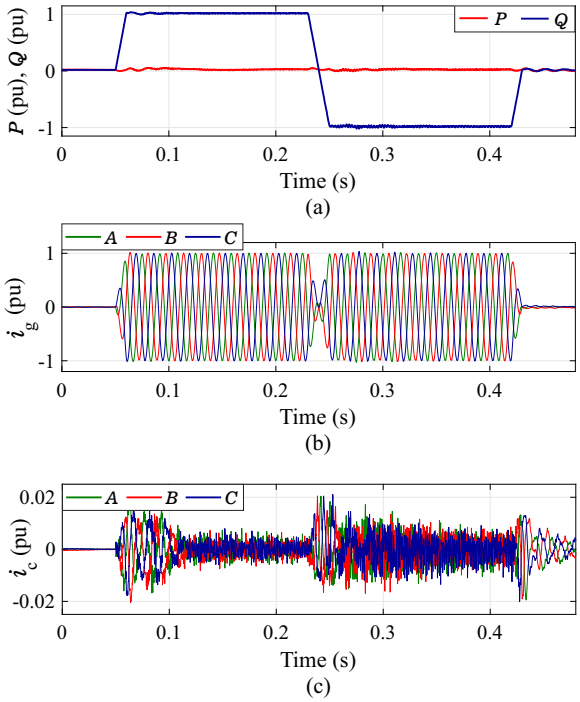
The instantaneous active and reactive powers are presented in Fig. 42 (a). As observed, the reactive power exchanged follows the reference profile. Moreover, the grid currents shown in Fig. 42 (b) presents a shape based on reactive power profile. Additionally, the grid current THD in both operation modes is lower than 3%. The circulating currents are presented in Fig. 42 (c). The circulating currents reach a ripple around 0.01 pu during

Figure 41 – SM capacitor voltages of the upper arm of MMC phase A in both inductive and capacitive reactive power operations: (a) Measured voltages; (b) Observed voltages; (c) Relative errors.



Source: Elaborated by the author.

Figure 42 – Dynamic behavior of HB-MMC in both inductive and capacitive reactive power operations: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents.



Source: Elaborated by the author.

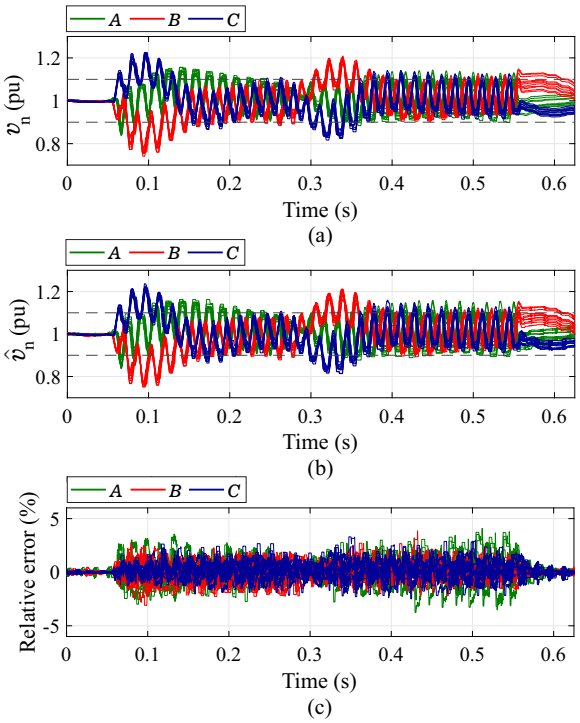
steady state, against 0.007 pu, when the measured capacitor voltages are employed in the control.

3.7.5 PSI- and NSI-LVRT

Positive and negative sequence current injections are considered in this case study for LVRT operation. The same operational conditions as defined in Section 2.3.1.4 are adopted.

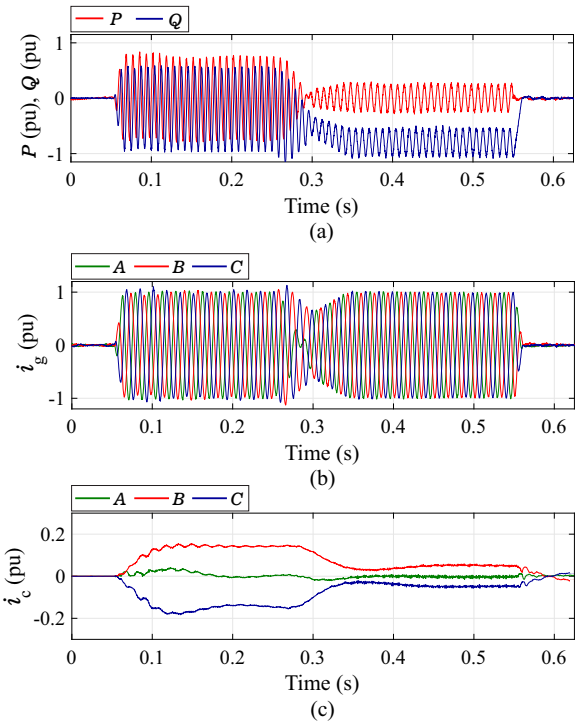
Measured and observed SM capacitor voltages for the three upper arms are presented in Fig. 43. As observed, the SM capacitor voltage ripple depends on the values of positive and negative sequence currents. Different ripples are observed in each phase due the unbalanced currents. It is important to remark that the lower arms have similar behavior. The maximum ripple in steady-state for the most stressed phase is slightly greater than the 10% range adopted. Moreover, this condition also occurs when the measured capacitor voltages are employed in the control. The relative errors between the measured and estimated values are within ± 5% in steady-state, as shown in Fig. 43 (c).

Figure 43 – SM capacitor voltages of the upper arm of MMC phase A during LVRT: (a) Measured voltages; (b) Observed voltages; (c) Relative errors.



Source: Elaborated by the author.

Figure 44 – Dynamic behavior of HB-MMC during LVRT: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents.



Source: Elaborated by the author.

The instantaneous active and reactive powers are presented in Fig. 44 (a). As observed, the instantaneous active and reactive power present oscillatory components at the doubled line frequency (120 Hz) during both PSI or NSI. Furthermore, the grid currents shown in Fig. 44 (b) are unbalanced and the stresses in the converter phases are different when both sequences are processed during MSI. Regarding the circulating currents presented in Fig. 44 (c), a dc value of 0.18 pu is observed for phase B when only NSI is processed. Furthermore, no significant variation is noted for the grid voltage dynamics compared to Figs. 29 (b) and (c), being hidden for simplicity.

3.8 Conclusions

In this chapter, a sliding-mode observer for MMC-based STATCOM systems was employed. The results show satisfactory response during both dynamic and steady-state operating conditions. The observer was adapted to NRM and CM operating modes during the converter initialization. A linear correction was proposed within the hysteresis band to reduce the chattering in observer dynamics. Moreover, the stability of the observer was

proven, using Lyapunov's direct method. Furthermore, the effect of the switching and sampling frequencies on the observer performance was evaluated, as well as the variation of the SM capacitance value.

The observer can be implemented in the existing controller and replace the capacitor voltage measurements for its observed voltages. This approach does not reduce the reliability of the system, since the high number of measured signals received by the controller of a traditional MMC raises concerns about random sensor failures. This reliability assessment is described in detail in the Chapter 5. The next chapter evaluates the proposed HB-MMC design and the observer adopted, considering the converter operation under SM failures.

4 On Converter Fault Tolerance in MMC-based STATCOM systems

Usually, MMC employ tens to hundreds of SMs. Due to the high number of components, concerns regarding reliability arise. In practice, the STATCOM system must operate for some years without interruption to replace damaged SMs. During the planned maintenance period, the damaged SMs are replaced. In view of this fact, the converter must be designed to operate with some fault-tolerance schemes (Sharifabadi et al., 2016). MMC fault-tolerance schemes have been investigated in many publications in recent years. For example, the search "fault tolerance in modular multilevel converter" in IEEE Xplore database leads to more than 200 results. In view of this fact, some works present the main aspects and perspectives for the MMC.

He, Yang and Wang (2020) present a comprehensive review of existing fault detection methods and fault tolerant strategies for MMC including dc-bus short-circuit faults and ac-side single line-to-ground faults. Farias et al. (2018) present a comparison and analysis of four redundancy strategies applied in MMC-based STATCOM systems. A review on the most relevant fault diagnosis methods and fault-tolerance strategies of the MMC-based HVDC systems is presented in (Liu et al., 2016). A comprehensive survey on the converter fault-tolerance strategies for the MMC-based HVDC systems is described in (Farias et al., 2020).

In view of the points aforementioned, the main proposed converter fault-tolerance schemes for MMC-based STATCOM systems are provided in this chapter, based on the available technical literature. Analytical expressions to determine the maximum number of SM failures in the MMC-based STATCOM systems are employed. Thereafter, the limitations of the main converter fault-tolerance schemes under SM failures are described and critically compared. Furthermore, the effect of the faulty SMs on the converter dynamics for different fault-tolerance strategies are evaluated. In this sense, the same parameters defined in Chapter 2 are employed, and only the closed-loop control with the sliding-mode observer is considered.

4.1 Faults in Modular Multilevel Converters

Failures in power semiconductor devices cause the MMC to operate displaced from the setting point or even to turn off the converter (Shao et al., 2016). Therefore, the converter fault tolerance is necessary. It is based on three steps: i) fault diagnosis; ii) bypassing of the faulty SMs; iii) converter fault-tolerance schemes. These three steps are

described in detail in this section. It is important to remark that the faults described below are focused on faults at the SM level.

4.1.1 Fault Diagnosis

An SM can experience faults in different components, such as IGBT modules, capacitors, control system or power supply. Indeed, the fault mechanisms depend on the kind of component and the technology employed. Therefore, the plastic IGBT module (PIM) is considered in this section, since this technology is mature and widespread in industry. These IGBT modules present both open-circuit failure mode (OCFM) and short-circuit failure mode (SCFM). The OCFM appears due to the bond-wire lift-off in PIM caused by over-temperature or aging. Usually, no additional serious damage is caused to the system due the protection scheme. On the other hand, SCFM are caused by wrong gate signals, overvoltage, or high temperature and could cause additional damage to other components in the circuit (Liu et al., 2015). Therefore, the efficient and fast fault detection methods are required. The fault detection approaches found in the literature can be divided into two main groups.

4.1.1.1 Hardware-based Methods

Employ redundant components or additional sensors. A failure can be detected if the behavior of the components is different from the redundant ones, or the additional sensors detect anomalous signals. Some fault detection methods with an additional sensor for each IGBT device or each half-bridge SM are presented in (Huang; Flett, 2007).

The hardware-based methods require additional sensors and signals, which increases the cost and the implementation complexity for MMC-based STATCOM, due to the high numbers of SMs. Therefore, the fault detection methods based on the existing measured variables in the original controllers are becoming a trend (Hui Liu; Poh Chiang Loh; Blaabjerg, 2013). In this view, the application of analytical methods is increased by the great advances in computational technology in recent decades (Shao et al., 2016).

4.1.1.2 Analytical Methods

The sliding-mode observer can be also employed to detect the OCFM and the faulty SM (Oates et al., 2015; Shao et al., 2013). The MMC operating condition is obtained by the differences between the observed arm current values and the measured arm current values. The operation status of each SM can be easy to access by comparing with a predefined threshold. However, each SM capacitor voltages must be measured. Moreover, the detection and diagnosis accuracy can be achieved only with a precise MMC model, which is difficult to comply due to system complexity. Similar features are presented in the SM fault detection based on Kalman filter (Deng et al., 2015).

An algorithm for real-time diagnosis of power semiconductor during both OCFM or SCFM has been proposed in Liu et al. (2015). Such algorithm provides information on the fault type and the affected phases. A fault detection method for multilevel converter based on the switching frequency analysis of the output phase voltages is presented in Lezana, Aguilera and Rodriguez (2009). This method is based on the principle that the magnitude becomes significantly larger after the occurrence of a fault due to the imbalanced cancellation of the switching frequency harmonics. However, the localization of the faulty module is complex to implement and easy to get the wrong diagnosis in a transient operation, especially with large number of SMs.

Some fault diagnosis methods use artificial intelligence-based techniques. The neural networks based on fast Fourier transform (FFT) (Khomfoi; Tolbert, 2007) and discrete Fourier transform (DFT) (Jiang et al., 2012) require only the output phase voltage measurements to detect the faulty SM. The major drawback of these three methods is the long training time for all the fault conditions, especially with large number of sample data. Moreover, those kinds of data are difficult to obtain.

Although the analytical methods are more sophisticated, the cost and hardware complexity are smaller than those required by the hardware-based methods. The comparison of SM fault detection methods are summarized in Tab. 9. The suitable choice of SM fault detection methods depends on design constraints such as system investment, the existing voltage and/or current measurements, and the detection performance. According to the MMC design, the voltage and current sensors needed for the SM fault detection methods may already be available. However, it is important to note that the SM capacitor voltage sensors $6N$ can be also denoted as additional sensors, since some approaches aim to eliminate the presence of such sensors.

Table 9 – Comparison among different SM fault detection methods. Adapted from (Liu et al., 2016)

Reference	Method	Measurements Signals	Fault Detection	Number of Sensors
(Huang; Flett, 2007)	Hardware-Based Method	SM Capacitor Voltages and Semiconductor Voltages	OCFM and SCFM	$6N + 6N$
(Shao et al., 2013)	Sliding-Mode Observer	SM Capacitor Voltages and Arm currents	OCFM	$6N + 6$
(Deng et al., 2015)	Kalman Filter	SM Capacitor Voltages and Arm currents	OCFM	$6N + 6$
(Liu et al., 2015)	Algorithm Method	SM Capacitor Voltages and Arm currents	OCFM and SCFM	$6N + 6$
(Lezana; Aguilera; Rodriguez, 2009)	Switching Frequency Analysis	Output Phase Voltages	OCFM and SCFM	3
(Khomfoi; Tolbert, 2007)	Fast Fourier Transform	Output Phase Voltages	OCFM and SCFM	3
(Jiang et al., 2012)	Discrete Fourier Transform	Output Phase Voltages	OCFM and SCFM	3

4.1.2 Bypassing of the Faulty SMs

When fast bypass activation is required, the fault identification and location can be performed in around 10 microseconds (Ødegård et al., 2016). In this sense, a suitable bypass structure must be employed to isolate the faulty SM. The bypass structure is strongly dependent on the semiconductor technology and the SM topology employed, which will be described in detail below. In addition, the bypass structure included in the converter SM is useful to implement some redundancy strategy. It is important to mention that the MMC market is mostly focused on HVDC systems, so many manufacturers use the existing SM solutions to perform STATCOM systems. Thus, the bypass structures presented below are often designed to meet the specific requirements of HVDC systems. In that way, mainly differences can be highlighted regarding the dc-link short circuit presented in HVDC system, which requires a fast switch (i.e., thyristor) to protect the SM devices.

4.1.2.1 Fault Mechanisms and bypass structures of PIM-based SMs

Most MMC designs are based on standard PIM for HB-SM. Therefore, the fault mechanism focused on the semiconductor devices S_1 and S_2 is demonstrated in Fig. 45. Moreover, the operating modes are summarized in Tab. 10. For the sake of simplicity, the bypass structure and the bleeder resistor are omitted. Furthermore, a generic MMC arm is considered. Notice that $q = 1$ refers to the ON state of the SM upper-switch (S_2). Firstly, assuming that no SM fault occurs, the arm current i_{arm} flows through D_2 and C, when $i_{arm} > 0$ and $q = 1$, and the SM capacitor is charged. On the other hand, if $q = 0$, the arm current flows through S_1, and the SM capacitor voltage remains stable. When $i_{arm} < 0$ and $q = 1$, the arm current flows through S_1 and C, discharging the SM capacitor. Finally, the SM capacitor voltage maintains stable and the arm current flows through D_1, if $q = 0$.

Figure 45 (a) shows an OCFM occurrence in S_2. As noted in Tab. 10, the SM operates as in no fault condition for all situations, except for $i_{arm} < 0$ and $q = 1$. Under such conditions, the arm current is forced to go through D_1 instead of S_2 and C. Similar behavior is noted when OCFM occurs in S_1, as shown in Fig. 45 (b). In this case, the arm

Table 10 – Four working regions of HB-SM in MMC for different operating conditions. Adapted from (Liu et al., 2016)

Arm	Gate	Arm Current Goes Through				
Current	Signal	No faults	Fig. 45 (a)	Fig. 45 (b)	Fig. 45 (c)	Fig. 45 (d)
$i_{arm} > 0$	$q = 1$	D_2 and C	D_2 and C	D_2 and C	S_2^* and C	S_1^*
$i_{arm} > 0$	$q = 0$	S_1	S_1	D_2 and C	S_2^* and C	S_1^*
$i_{arm} < 0$	$q = 1$	S_2 and C	D_1	S_2 and C	S_2^* and C	S_1^*
$i_{arm} < 0$	$q = 0$	D_1	D_1	D_1	S_2^* and C	S_1^*

* The device is short-circuited.

current is forced to go through D_1 and C instead of S_1, as in nominal operation.

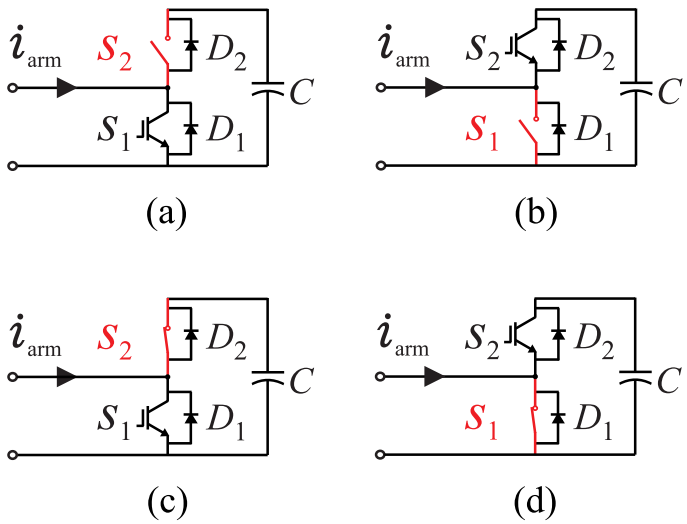
The SCFM occurrence in S_2 is illustrated in Fig. 45 (c). As shown in Tab. 10, the arm current flows through the short-circuited S_2 and C for all states. Under such conditions, since S_1 is turned on, the SM capacitor discharges through the loop formed by S_1, the short-circuited S_2 and the capacitor C, if no protective action is taken. Due to the small time constant of the capacitor discharging loop, the SM capacitor discharges very quickly, leading to large short-circuit current within the faulty SM. The surge currents can be as high as 500 kA (Ladoux; Serbia; Carroll, 2015), which can lead S_1 to fail in open-circuit. Thereafter, the SM capacitor is charged for $i_{arm} > 0$, and discharged for $i_{arm} < 0$.

Similar behavior as noted when the SCFM occurs in S_1, as shown in 45 (d). In this case, since S_2 is turned on, the SM capacitor discharges through the loop formed by S_2, the short-circuited S_1 and the capacitor C, if no protective action is taken. Therefore, if the S_2 is led to fail in open-circuit, the arm current always flows through the short-circuited S_1 and the SM capacitor voltage is brought to zero due the bleeder resistor.

As noted, the surge current appears in the faulty SM rather than flowing through the whole MMC arm or phase during the SCFM. Moreover, the SM capacitor voltage cannot be controlled during the OCFM, leading to under-voltage or overvoltage conditions (Liu et al., 2015). Therefore, the faulty SM needs to be bypassed by the action of overcurrent protection devices, maintaining the operation of the system without interruption.

In the event of a SCFM, a significant damage can be expected at the point of failure, which may cause the semiconductor to explode, interrupting current flow. Although surge-limiting inductors can be connected between the upper switch and the SM capacitor,

Figure 45 – Failure configurations in HB-SM: (a) OFCM in S_2; (b) OCFM in S_1; (c) SCFM in S_2; (d) SCFM in S_1.



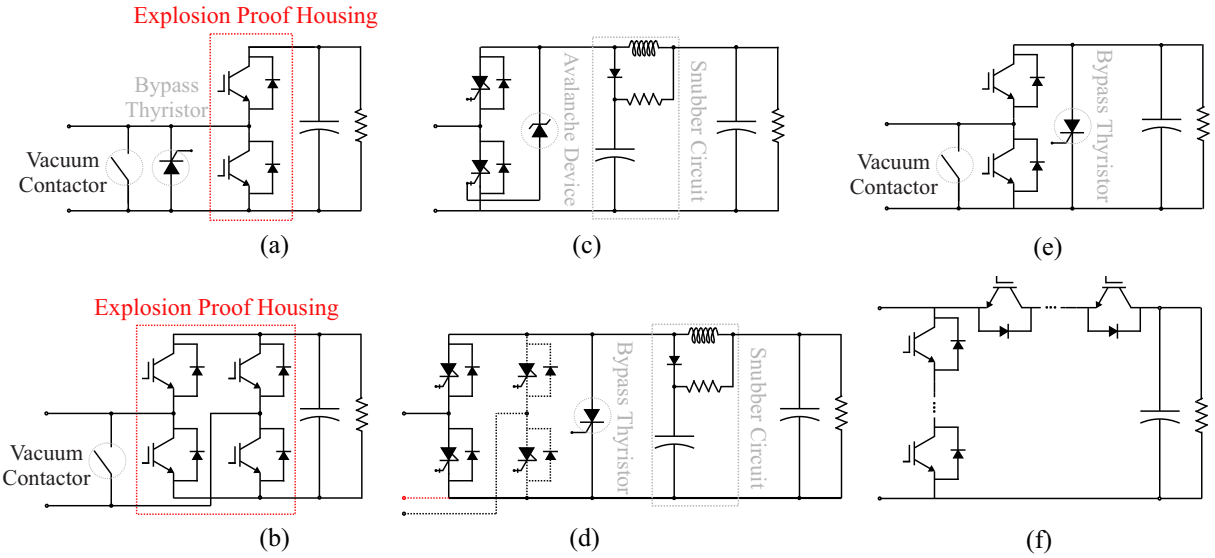
Source: Elaborated by the author.

the current is still high enough to cause the explosion of the device (Ladoux; Serbia; Carroll, 2015). In addition, this solution leads to an increase in the commutation inductance, which is a drawback. Therefore, when PIM is employed, a commonly adopted solution employs an explosion proof housing for the SMs as developed by the Frauenhofer Institute (Billmann; Malipaard; Gambach, 2009). This housing damps the explosion and contains the plasma during the time needed for the SM capacitor to discharge. Under such conditions, a mechanical bypass switch (vacuum contactor) is activated to guarantee the SM current continuity. Some manufacturers, such as Siemens, GE and Alstom present solutions based on half- and full-bridge SMs, as shown in Figs. 46 (a) and (b), respectively (Davies et al., 2017; GE, 2017; Hassan, 2011).

As noted in Fig. 46 (a), a press-pack thyristor is connected in parallel with the vacuum contactor to protect the low-switch diode, if a dc-link short-circuit occurs. The diodes of PIM cannot handle the surge currents. This fact arises from the construction of standard PIM, which include the diodes inside the power module. Indeed, PIM is mainly designed for motor drive applications, where the current stresses in the diodes are not severe. In this way, the thyristor must provide a fast bypass (turn-on time of few microseconds), compared with the vacuum contactor (turn-on time of tens of milliseconds).

On the other hand, since the thyristor cannot handle ac currents, the vacuum contactor assumes the arm current, which can handle the rated current without any cooling (Wang et al., 2017). It is important to remark that the selected thyristor is a high-voltage device, which must present a current rating compatible with the surge currents and forward

Figure 46 – Different bypass structure realizations for: (a) PIM-based half-bridge SMs; (b) PIM-based full-bridge SMs; (c) IGCT-based half-bridge SMs; (d) IGCT-based half- or full-bridge SMs; (e) PPI-based half-bridge SMs; (f) PPI-based half-bridge SMs without bypass structure.



Source: Elaborated by the author.

voltage drop much lower than the diodes (Bordignon et al., 2016). Moreover, the thyristor is not required in Fig. 46 (b), since the dc-link short-circuit handling capability is inherent of the full-bridge topology.

4.1.2.2 Fault Mechanisms and bypass structures of PPI- and IGCT-based SMs

Regarding press-pack IGBT (PPI) and IGCT devices, the use of discrete devices allows selecting diodes that can handle the surge currents during dc-link short-circuits. Moreover, PPI and IGCT devices have inherent stable SCFM, which avoids the bypass structure requirement (Ladoux; Serbia; Carroll, 2015). However, potential problems can occur if theses devices are not triggered, as might happen in the event of loss of the gate-drive power supply. Since no bypass structure is required, the semiconductors would fail by overvoltage, causing the link-capacitor to fail first (explosion). One possible solution is to connect an avalanche device (pressure-assembled) from the positive capacitor terminal to the gate terminal of the low-side device to force a SCFM and short-circuit the ac terminals. In addition, a snubber circuit is employed to ensure a reduced di/dt and overvoltage protection. This approach is adopted by ABB for IGCT-based half-bridge SMs (Ladoux; Serbia; Carroll, 2015), as shown in Fig. 46 (c).

The stored energy in some high-power applications is large enough ($>$ 100 kJ per SM) to compromise the installation during the SM capacitor discharges due to the risk of semiconductor housing rupture, external arcing, capacitor explosion or electro-mechanical rupture of electrical connections [1] (Wikström; Ødegård; Baumann, 2019). Therefore, one possible solution for devices with inherent SCFM is to connect a sacrificial bypass thyristor in parallel with the SM capacitance (Ødegård et al., 2016). If a failure occurs, the thyristor is fired to assume the capacitor discharge current. Thereafter, the thyristor fails in a long-term stable SCFM and the SM is bypassed through the current path created by the freewheeling diodes and the sacrificial bypass thyristor. This approach was proposed by ABB for IGCT-based half- or full-bridge SMs (Ødegård et al., 2016), as shown in Fig. 46 (d). The main drawback of this solution is the power losses in the diodes of the faulty SM. Therefore, RXPE has proposed the use of an additional bypass vacuum contactor for the PPI-based half-bridge SMs, as shown in Figs. 46(e), to reduce the power losses (Bordignon et al., 2016).

ABB and C-EPRI also employ half-bridge SMs without any bypass structure, as shown in Fig. 46(f) (Ødegård; Monge, 2017; C-EPRI , 2017). Series-connected PPI devices are employed in the SM to avoid the problem of surge currents during SCFM. When one device fails, the other IGBTs handle the SM capacitor voltage. Additional devices must be included to provide redundancy, as in the earlier two- and three-level converters (Jacobson

[1] For a sense of the destructive potential, this energy is comparable to dropping the bypass thyristor from the top of Mount Everest.

et al., 2010). Therefore, the redundancy is implemented at the device level, instead of SM level.

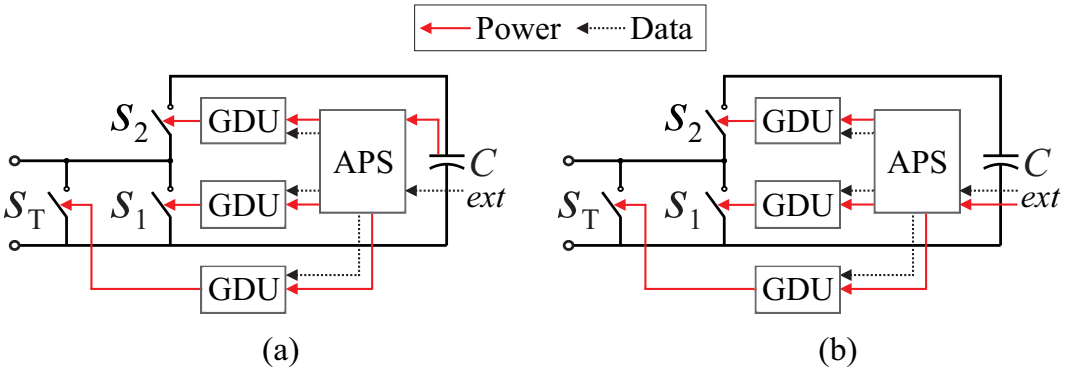
4.1.2.3 Auxiliary Power Supplies for SMs

The HB-SM contains two gate-drive units (GDU), i.e. one for each active power semiconductor device. Each of these gate drivers requires a certain amount of power both during conduction and switching operations of the active device, and when the device, for some reason, is idle. Regarding IGBT-based HB-SMs, the necessary average value of auxiliary power is of the order of 1 W, whereas in the case of IGCT-based HB-SMs this value may be approximately 50 W (Sharifabadi et al., 2016). In general, the gate drive requires a low-power supply providing in the range of 1-100 W at a voltage of 15-25 V.

There are two common auxiliary power supply (APS) solutions. One approach is to supply this power from the SM capacitor on a floating potential (also called internal APS). The second option is to take the power from a central power source with the same ground reference as that of the entire system (also called external APS). Figure 47 illustrates the two APS sources based on HB-SM (Heinig et al., 2022). Regarding HV applications, the best option is to take the power from the SM capacitor. The reason for this choice is that the SM capacitor follows the electric potential of the APS, such that a galvanic isolation of several tens or hundreds of kV is not necessary, and the isolation voltage is a few kV. On the other hand, for MV applications in the range of 1–52 kV, several external APS solutions have been reported (Heinig et al., 2022).

A big advantage of external APS is the black start capability, where auxiliaries could be powered before the main circuit. Therefore, access to control equipment, sensors, and monitoring data is possible without the need for complicated start-up procedures (Heinig et al., 2022). Moreover, external APS is also important to the bypass structure. Assuming that the bypass thyristor is triggered, the faulty SMs must stay bypassed until

Figure 47 – Auxiliary power supply for a half-bridge SM: (a) Internal APS; (b) External APS.



Source: Adapted from Heinig et al. (2022).

the next scheduled shut-down for maintenance. During the bypass of the SM, the bleeder resistors are expected to discharge the SM capacitor. Therefore, the bypass of the faulty SMs is maintained even when the SM capacitor discharges. On the other hand, if the internal APS is applied, one possible approach is to employ a mechanical bypass switch in parallel with the bypass thyristor, which ensures a permanently bypass of the faulty SMs even when the SM capacitor discharges (Wang et al., 2017).

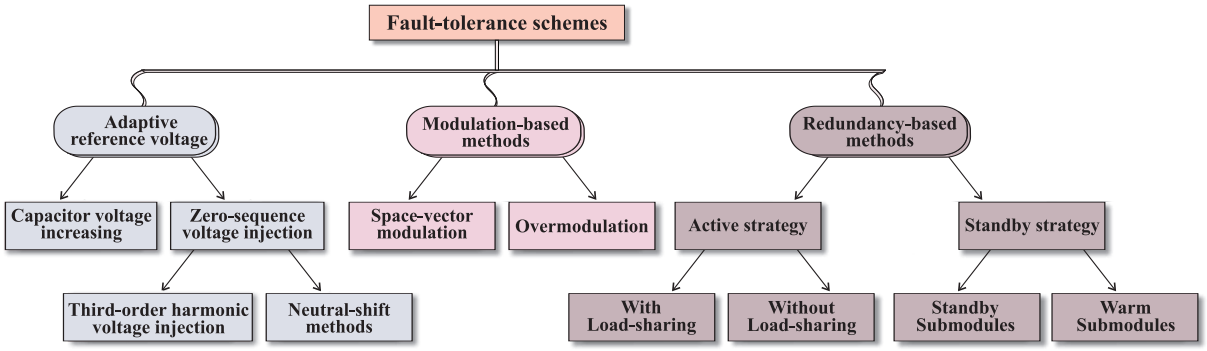
4.1.3 Converter Fault-Tolerance Schemes

The objective of the converter fault-tolerance control system is to overcome the presence of faulty SM and restoring the stability of the power converter with acceptable performance level (Abdelsalam; Marei; Tennakoon, 2017). In general, there are two bypass schemes for the MMC under SM failure conditions (Yang et al., 2019). In this first solution, the faulty SMs are bypassed as well as an equal number of SMs in other MMC arms, to keep the MMC symmetrical operation. The second approach is carried out bypassing only the faulty SMs and then the MMC operates in asymmetric state. A notable advantage of the asymmetric operation is the use of all healthy SMs in the MMC operation. However, this approach results in asymmetry in the synthesized voltage of the faulty phase. In the absence of one or more SMs, some MMC fault-tolerance method must be employed, reconfiguring the MMC control or compensating the faulty SMs by a redundant one. These methods are classified in this work in three types: adaptive reference voltage, modulation-based methods and redundancy-based methods. In this sense, the main fault-tolerance schemes for HB-MMC are summarized in Fig. 48.

4.1.3.1 Adaptive Reference Voltage

The main adaptive reference voltage approaches are: capacitor voltage increasing (CVI) and zero-sequence voltage injection (ZSVI).

Figure 48 – Overview of the main fault-tolerance schemes applied to MMC-based STATCOM systems.



Source: Elaborated by the author.

The CVI method is one of the most straightforward MMC fault-tolerance methods. This approach is based on the voltage increase of one or more healthy SMs in the faulty arm to compensate the missed voltage capacity (Abdelsalam; Marei; Tennakoon, 2017; Alharbi; Isik; Bhattacharya, 2019). The number of levels at the converter voltage output is reduced while the overmodulation is avoided (Farias et al., 2018). Since MMC-based STATCOM systems have been built with tens to hundreds of SMs, reducing the output voltage levels would be an economic solution. Nevertheless, in practical applications, the safe operating area of the SMs is generally 50-60% of the semiconductors blocking voltages (ABB, 2017). Therefore, the CVI is limited by the maximum voltage stresses at the semiconductor devices and SM capacitors.

Among all methods injecting zero-sequence voltage to balance output voltages, the neutral-shift (NS) and the third-order harmonic voltage injection (THVI) methods should be highlighted. The NS method adjusts the angles between the phase voltages in such a way that all the healthy SMs are utilized, the line-to-line voltages are balanced, and the amplitude of line voltages is maximized (Yang; Qin; Saeedifard, 2016). The essence of the NS method is to inject a fundamental zero-sequence voltage (FZSV) based on phasorial calculation. The ac-side voltages of the converter with respect to the midpoint of its dc-side are regulated to be unbalanced. However, the three-phase line-to-line voltages of the converter are maintained as a balanced set, as shown in Fig. 49 (a). Thus, the amplitude of three-phase voltages of the converter should be proportional to the number of the remaining operating SMs in corresponding phases, which limits the converter output voltage (Sun et al., 2016). The NS approach can be applied as MMC fault-tolerance method by reference modification, as described by Das et al. (2016).

The THVI is an attractive approach for MMC control, due to the high dc-side voltage utilization ratio (Li; Fletcher; Williams, 2016). However, the THVI approach can only be considered a MMC fault-tolerance scheme if the converter is initially designed to operate with sinusoidal PWM modulation, maintaining the linear modulation region after implemented. Additionally, the challenge is to obtain the optimal magnitude and phase of the THVI (Guo et al., 2018a). Moreover, THVI has a significant impact on the SM voltage fluctuations of the MMC (Zhao et al., 2019). Its principle is presented in Fig. 49 (b).

4.1.3.2 Modulation-Based Methods

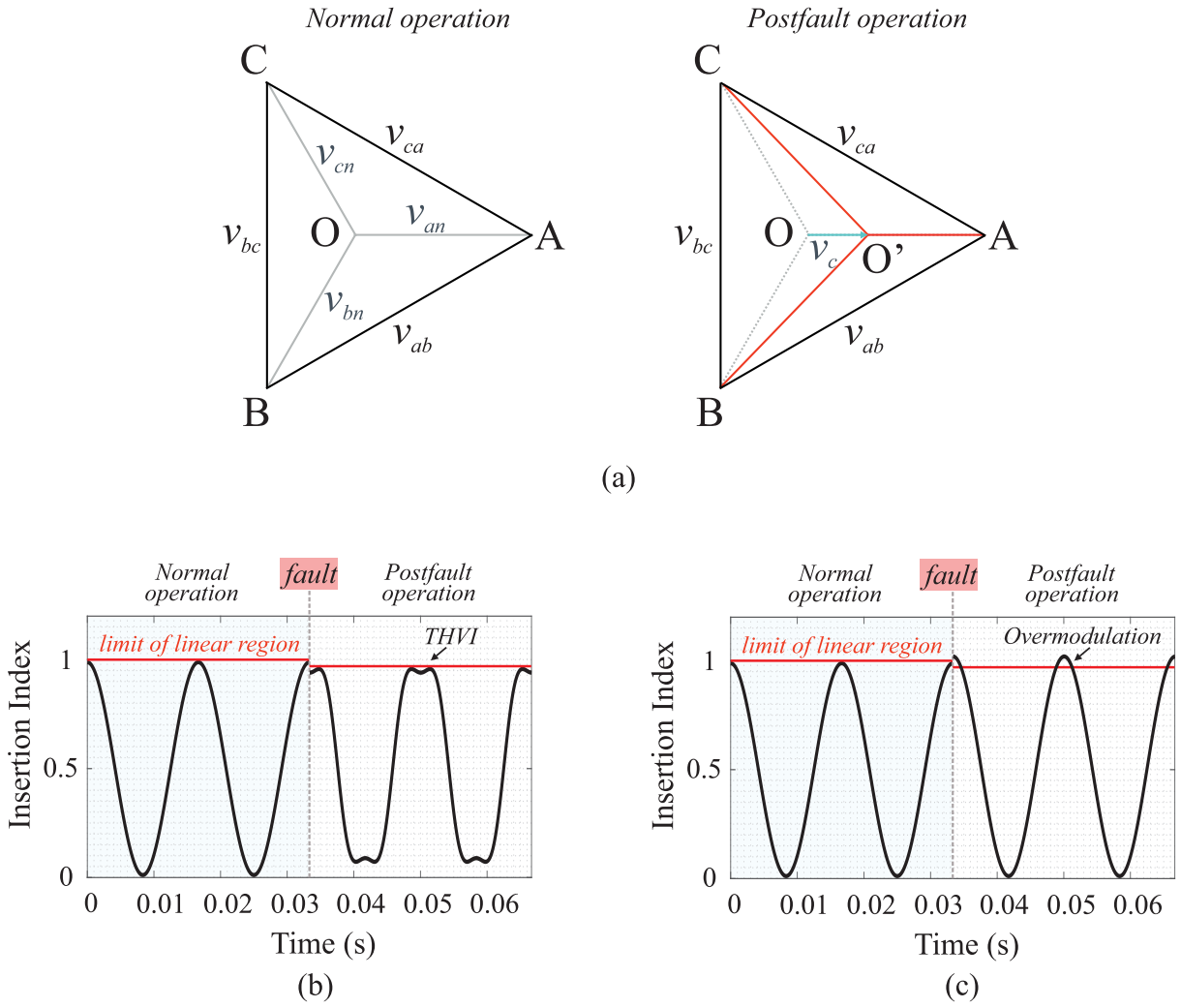
Another alternative to operate the converter under faulty SM condition is modifying the converter modulation scheme (Aleenejad; Mahmoudi; Ahmadi, 2016). These approaches can be sorted into space-vector modulation (SVM) and overmodulation methods.

The presence of redundant switching states is a well-known characteristic of multilevel converters. Through space-vector modulation, these states can be optimized. Zang et al. propose a fast SVM algorithm to control the converter under faulty conditions,

which can produce a three-phase balanced line-to-line voltage, as described in (Yi Zang et al., 2006). SVM methods able to insert an external dc offset to the faulty converter phases are presented in (Aleenejad; Mahmoudi; Ahmadi, 2016). These studies are performed for five- and seven-level CHB, which can be extended to low-level MMC application (Aleenejad; Mahmoudi; Ahmadi, 2016). However, the SVM techniques are quite complex for a high number of SMs.

MMC-based STATCOM systems are usually designed to operate in the converter linear region, which implies that the peak voltage in the ac-side should be lower than the dc-side voltage (López et al., 2015). However, the ac fundamental component of the voltage can be increased beyond this limit through overmodulation strategies, as shown in Fig. 49 (c). Since this voltage command is permanently beyond the limits (e.g. post-fault operation), it cannot be physically produced by the MMC. Therefore, operation in the overmodulation region can increase the THD in the output current (López et al., 2015).

Figure 49 – Operating principle of fault-tolerance methods: (a) Neutral-shift; (b) THVI; (c) Overmodulation.



Source: Adapted from Farias et al. (2020).

However, the THD in MMC-based STATCOM system might not be an issue, due to the large number of series-connected SMs. Additionally, Cupertino et al. (2019b) demonstrate that the MMC operating as STATCOM presents a notable inherent fault tolerance in the overmodulation region.

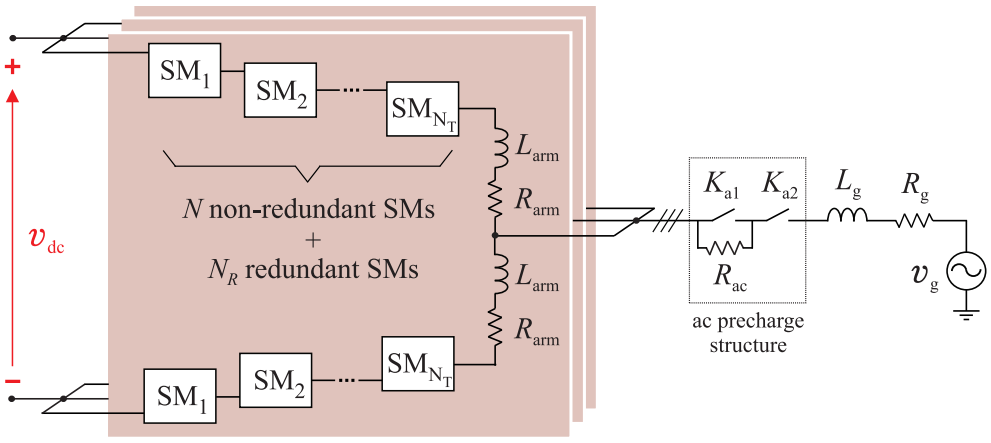
4.1.3.3 Redundancy-Based Methods

A redundancy strategy might be used to ensure that the converter remains operating without affecting the overall performance (Davies et al., 2017; Tu; Yang; Wang, 2019). Redundancy strategies can be implemented through N_R redundant SMs in the converter structure, as illustrated in Fig. 50. Therefore, the total number of SMs per arm becomes N_T, where $N_T = N + N_R$. In general, the redundant SMs can operate in active mode or standby mode.

The redundant SMs operate "actively". Essentially, there is no difference between the redundant SMs and non-redundant SMs. The MMC arm continues to operate as long as the number of healthy SMs is higher than N. This redundant mode can operate on active redundancy without load-sharing (AR) or active redundancy with load-sharing (ALR) (Chen; Yu; Li, 2019). A load-sharing rule dictates how stress or load is redistributed to the surviving components after a component fails or degrades within the system. Active redundant SM schemes are preferred in converter fault-tolerance operation for medium or low-voltage application (Xiao et al., 2019). The advantages of these active reserve methods are higher SM utilization ratio, no additional charging time for reserve SM and improved dynamic performance (Yang; Tang; Wang, 2018; Xiao et al., 2019). All these factors lead to the broad acceptance of active reserve methods in medium and low-voltage applications.

The redundant SMs are bypassed and initially discharged. When failures occur, the corresponding faulty SMs are bypassed from the MMC arm, and redundant SMs

Figure 50 – Schematic of the three-phase MMC-based STATCOM considering N_R redundant SMs.



Source: Elaborated by the author.

are inserted (Tu; Yang; Wang, 2019). Therefore, the standby redundancy (SR) approach, which involves bypassing and discharging the redundant SMs until operational, offers the advantage of minimal converter power losses. This makes it particularly suitable for hot-standby devices like STATCOM. However, an extra power supply is required for the redundant SM, since the capacitor is initially discharged in standby SMs (Liu et al., 2016). Another issue arises when a standby SM fails, since the failure can only be detected if the SM is operating. Moreover, this strategy results in the worst performance for dynamic behavior, since the charging process of the standby SMs affects the SM voltage and grid current (Farias et al., 2018).

To overcome the charging process of the standby SMs, the warm redundant SMs that work in voltage balance state under normal operation are presented in reference (Yang et al., 2019). Therefore, the redundant SMs can quickly replace the faulty SMs without significant transients. Moreover, the power losses of the redundant SMs are lower than those in active redundancy.

Theoretical analysis of the redundant sharing among the converter arms is described in (Guo et al., 2018b). As advantages, for the same reliability requirements, this strategy requires less redundant SMs. However, reconfiguration switches are required (i.e. thyristors), which increases the implementation complexity.

All the redundancy techniques have advantages in relation to converter reliability, besides ensuring symmetrical operation in post-fault condition. In addition, redundancy results in an inherent extra power that might be used in emergency situations (Konstantinou; Ciobotaru; Agelidis, 2012).

4.2 Comparison of MMC Fault-Tolerance Schemes

In this section, the limitations of the main converter fault-tolerance schemes in the occurrence of SM failures are described and critically compared.

4.2.1 Adaptive Reference Voltage

In the CVI method, the utilization ratio of the SM is improved effectively (Liu et al., 2016). The synthesized voltage remains unchanged and the SM capacitor voltages of the operating SMs are increased. Therefore, the following relation is obtained $(N - N_f)V_f^* \geq NV^*$, where N_f is the number of SM failures. Assuming $V^* = f_{us}V_{svc}$, such relation can be rewritten as:

$$(N - N_f)f_{us,f}V_{svc} \geq Nf_{us}V_{svc}. \tag{4.1}$$

where $f_{us,f}$ is the utilization factor after the SM failures. Therefore, the number of failures allowed by CVI method is given by:

$$N_{f,CVI} \leq \left(1 - \frac{f_{us}}{f_{us,f}}\right) N. \tag{4.2}$$

As listed in Tab. 4, typical values of the utilization factor are $50\% \leq f_{us} < 55.5\%$. Therefore, there is a safe operating zone within these limits that ensures the service continuity even during SM failures, as shown in Fig. 51. Furthermore, the operating zone of the converter can be extended for $f_{us,f} > 55.5\%$, which increases the operating voltage of the SMs. Under such conditions, the increased SM operating voltages should be moderated due to possible damage caused to the SM devices such as IGBTs and capacitors. It is important to remark that the extended zone of operation can be used in an emergency situation, ensuring an uninterrupted operation of the converter until the next scheduled maintenance.

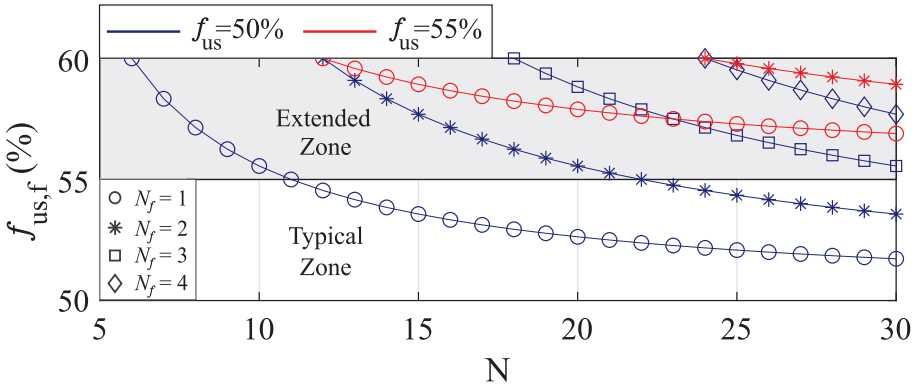
The dc-link voltage given in (2.44) can be rewritten as $V_{dc} = NV^*$. Alternatively, such relation can be described by the maximum number of SM failures allowed in the MMC:

$$V_{dc,f} = (N - N_f)V^*. \tag{4.3}$$

If the MMC is designed to operate with sinusoidal PWM modulation in steady state, the phase-to-neutral voltage synthesized by the converter is $\widehat{V}_{sn} = V_{dc}/2$. On the other hand, if the MMC operates with a THVI scheme under post-fault condition, $\widehat{V}_{sn} = V_{dc,f}/\sqrt{3}$ can be reached (Ilves et al., 2014). Under such conditions:

$$\frac{V_{dc,f}}{V_{dc}} = \frac{(N - N_f)V^*}{NV^*} = \frac{\sqrt{3}}{2}. \tag{4.4}$$

Figure 51 – Operating zone of the MMC-based STATCOM considering the CVI fault-tolerance scheme.



Source: Elaborated by the author.

Thus, the maximum number of SM failures is:

$$N_{f,THVI} = \left(1 - \frac{\sqrt{3}}{2}\right) N. \tag{4.5}$$

From (4.5), the THVI method allows about 13% of SM failures in post-fault operation. However, it is noteworthy that the initial design of the converter operating with the THVI method is more interesting, as detailed in Chapter 2.

According to (Xiao et al., 2020), the number of failures allowed by NS method is given by:

$$N_{f,NS} \leq N \left[1 - (1 + \delta_m)\left(\frac{1}{2} + \frac{\widehat{V}_g}{V_{dc}}\right)\right], \tag{4.6}$$

where δ_m is the modulation margin in practical application. As noted, the converter fault tolerance of the NS method is related to the modulation margin. Therefore, as described for the THVI methods, the initial design of the converter operating with the NS method is more interesting.

4.2.2 Modulation-Based Methods

The SVM schemes have an interesting feature for hot-standby devices as STATCOM due to the reduced switching loss of the converter. Nevertheless, the reduced output voltage in post-fault condition is the common drawback for these schemes (Zhang et al., 2014). Moreover, in an MMC with a large number of SMs (N > 20), it is difficult to implement the SVM schemes (Dekka et al., 2017).

The operation in the region of overmodulation is not desired under normal conditions. Indeed, long periods of operation in the overmodulation region should be avoided due to reduced power quality. However, there are exceptional cases in which MMC could be forced to operate in this mode. These would include transient conditions or quasi-permanent conditions, such as the failure of one or more SMs of the MMC (López et al., 2015). Moreover, MMC operating as STATCOM presents a notable inherent fault tolerance in the overmodulation region (Cupertino et al., 2019b), which could be complementary to another fault-tolerance method.

Due to the described limitations of the SVM and overmodulation schemes in MMC-based STATCOM systems under faulty SM conditions, such methods are disregarded in the next sections.

4.2.3 Redundancy-Based Methods

Regarding redundancy-based methods, the redundant SMs increase the converter reliability at the cost of increased component investment and control complexity (Xiao et al., 2020). Therefore, the maximum allowed number of failures in these methods depends only on the cost related to the implementation of redundant SMs. In this sense, the next chapter presents a methodology to provide a trade-off between cost and reliability of the converter.

Furthermore, the power losses of the warm redundant SMs are higher than the spare redundant SMs, imposing some practical limitations on its application. In view of the points aforementioned, the next sections aim to evaluate the effect of the faulty SMs on the MMC dynamics, considering only the CVI, AR, ALR and SR methods.

4.3 Control and Modulation Under Faulty SMs

Since a fault-tolerance scheme is employed, some equations described in Chapter 2 must be adapted. When SM failures occur, the maximum number of "on-state" SMs in each arm during a fundamental period is equal to the number of operating SMs, defined as $N_o = N_T - N_f$. Under such conditions, the total number of operating SMs in the converter is $6N_o$. Therefore, the average voltage is computed by:

$$v_{avg} = \frac{1}{6N_o} \sum_{n=1}^{6N_o} v_n, \tag{4.7}$$

The average voltage reference v^*_{avg} is dependent on the redundancy strategy employed. For AR or SR strategies, the average reference voltage is maintained even during SM failures as:

$$v^*_{avg} = \frac{V_{dc}}{N}, \tag{4.8}$$

On the other hand, when CVI or ALR strategies are employed, the SM voltage reference at the failed arms is increased to compensate the faulty SMs. Since only the faulty SMs are removed from the main circuit, the capacitor voltages of the remaining SMs are increased by the gain $\frac{N_T}{N_T - N_F}$, where $N_T = N$ for CVI method. Moreover, the average voltage reference v^*_{avg} is calculated by:

$$v^*_{avg} = \frac{1}{N_T} V_{dc}, \tag{4.9}$$

Regarding the PSC-PWM, the angular displacement of the carriers is calculated according to the number of operating SMs. Therefore:

$$\theta_{u,n} = 2\pi\left(\frac{i-1}{N_o}\right) \tag{4.10}$$

$$\theta_{l,n} = \theta_{u,n} + \beta_c, \tag{4.11}$$

where $i = 1, 2, ..., N_o$. Aiming to maintain the $(2N+1)$-level modulation, the angle β must be adapted, since the number of operating SMs can be odd or even during the converter operation. Thus:

$$\beta_c = 0, \quad \text{if } N_o \text{ is odd} \tag{4.12}$$

$$\beta_c = \frac{\pi}{N_o}, \quad \text{if } N_o \text{ is even} \tag{4.13}$$

Finally, considering that the THVI is initially inserted in the modulation, the normalized reference signals per phase can be defined as:

$$v^*_{u,n} = \frac{v^*_b}{v^*} + \frac{v^*_c}{N_o v^*} - \frac{v^*_s}{N_o v^*} + \frac{v^*_{3s}}{N_o v^*} + \frac{1}{2}, \tag{4.14}$$

$$v^*_{l,n} = \frac{v^*_b}{v^*} + \frac{v^*_c}{N_o v^*} + \frac{v^*_s}{N_o v^*} - \frac{v^*_{3s}}{N_o v^*} + \frac{1}{2}. \tag{4.15}$$

4.3.1 Fault-Tolerant Communication Networks

Regarding the fault-tolerant operation of the MMC communication network, it is important to note that both centralized and decentralized architecture presented in this work have an inherent fault-tolerant operation. As observed in Figs. 22 and 35, a failure in one or more SM has no effect in the communication between the remaining SMs and the main controller, since the data is exchanged directly between the SMs and the main controller, even in the case of the SM-level decentralized architecture. On the other hand, if the number of SM is extremely high as in HVDC application, a ring configuration (e.g. EtherCAT network) can be preferred aiming to reduce the length requirement for fiber-optic cables and the number of communication port in the communication hubs (Sharifabadi et al., 2016). However, only a moderate number of SMs is adopted in the presented analysis and such communication network is beyond the scope of this work.

4.4 Results

4.4.1 Simulation Results

This section aims to validate the MMC-based STATCOM considering four different fault-tolerance schemes. Since the sliding-mode observer is already validated for dynamic

and steady-state performances, the performance under SM failures is evaluated in this section. The observer is employed and the SM capacitor voltages are measured only to validate the performance. The same parameters presented in Tab. 5 are chosen. Moreover, -1 pu of reactive power in converter capacitive operation is considered.

For the sake of simplicity, the results shown are based on the C_{45} solution, which employs semiconductor voltage of 4.5 kV. Moreover, a redundancy factor of 10% is initially employed. Under such conditions, the AR, ALR and SR methods present $N_R = 1$, since $N = 11$ is employed for the C_{45} solution. A failure of 1 SM in the upper arm of MMC phase A is simulated at $t = 0.1s$, which S_1 is permanently turned on by $q = 0$. Regardless of the chosen failure detection method, the detection and isolation of the faulty SM needs around few microseconds until some milliseconds. Under such conditions, a delay of $1/f_g = 16.67$ ms is considered for the detection and isolation of the faulty SM. Then, the vacuum contactor is activated and the adjustment of the carrier angular displacement is performed, according to (4.11) and (4.13).

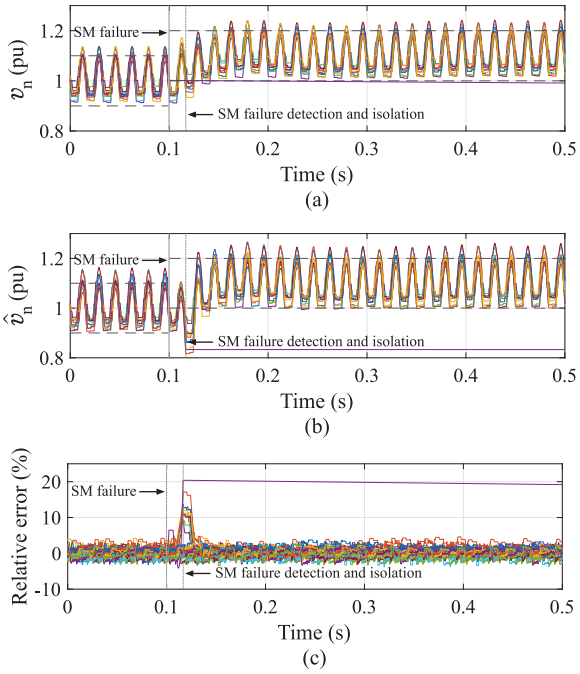
4.4.1.1 MMC Dynamics Considering Capacitor Voltage Increasing

Measurements and estimates of the SM capacitor voltages in pu are shown in Figs. 52 (a) and (b), respectively. Initially, the SM capacitor voltages are in nominal operation with average voltage value of 1 pu. When a failure occurs, the capacitor voltages of the remaining SMs are increased by the gain $\frac{N}{N-N_F}$, to compensate the faulty SMs in each arm. Therefore, the average measured voltage is around 1.1 pu in steady-state, leading to an utilization factor of $f_{us,f} = 55\%$.

As noted, 16.67 ms is associated with detecting SM failure and transmitting this information to the observer. Within this time interval, the observer continues to estimate the faulty SM voltages, as well as the remaining SM voltages, based on the configuration previous to the failure. This leads to errors in the observed voltages of the SM in operation, as shown in Figs 52 (c). Once the SM failures are acknowledged, the observer neglects the faulty SMs and the relative errors of the remaining SMs converge to pre-failure values. As observed, during the steady-state operation, the relative errors between the measured and estimated values are within $\pm$ 5%, except for the faulty SM. In this case, the relative error for the faulty SM differs due to the time interval associated with the SM failure detection, and the bleeder resistor R_b present in each SM. Similar behavior is noticed for the next analysis considering different fault-tolerance methods.

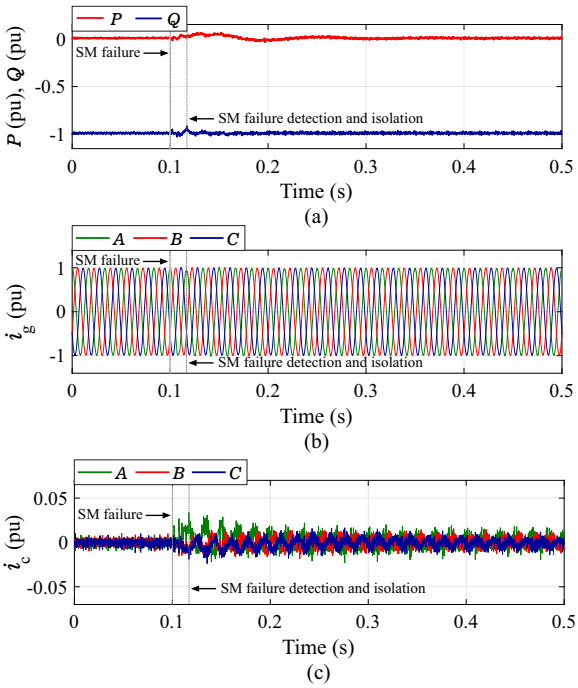
The instantaneous active and reactive powers are presented in Fig. 53 (a). When a failure occurs, active power is required by the converter, since the remaining SM capacitors should be charged. Moreover, the grid and circulating currents are shown in Figs. 53 (b) and (c), respectively. The SM failure generate a transient response in the current dynamics, which is extinguished after approximately 100 ms. Moreover, the circulating currents reach

Figure 52 – SM capacitor voltages of the upper arm of MMC phase A considering CVI method: (a) Measured voltages; (b) Observed voltages; (c) Relative errors.



Source: Elaborated by the author.

Figure 53 – Dynamic behavior of HB-MMC considering CVI method: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents



Source: Elaborated by the author.

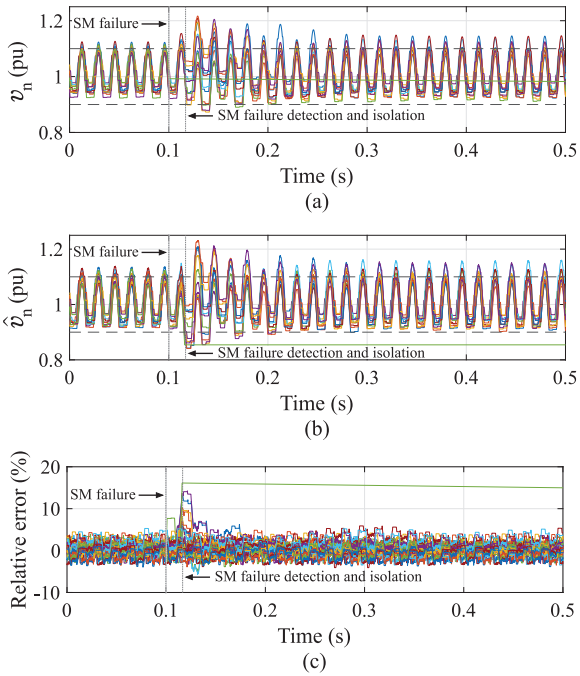
around 0.03 pu during transient operation.

4.4.1.2 MMC Dynamics Considering Active Redundancy without Load-Sharing

Figures 54 (a) and (b) show the measurements and estimates of the SM capacitor voltages, respectively. Initially, the SM capacitor voltages are in nominal operation with average voltage value of 1 pu. When a failure occurs, the reference voltage of the SMs is maintained constant, which results in smaller transient when the failures happen. The transient observed is justified by the adjustment of the carrier angular displacement, which is made dynamically according to (4.11) and (4.13). It is important to remark that the capacitor voltage ripple is increased after the failure, which can be compared with the result without redundant SMs. Moreover, the relative errors between the measured and estimated values are illustrated in Fig. 54 (c). As noted, except for the faulty SM, the relative errors are within ± 5% during steady-state operation.

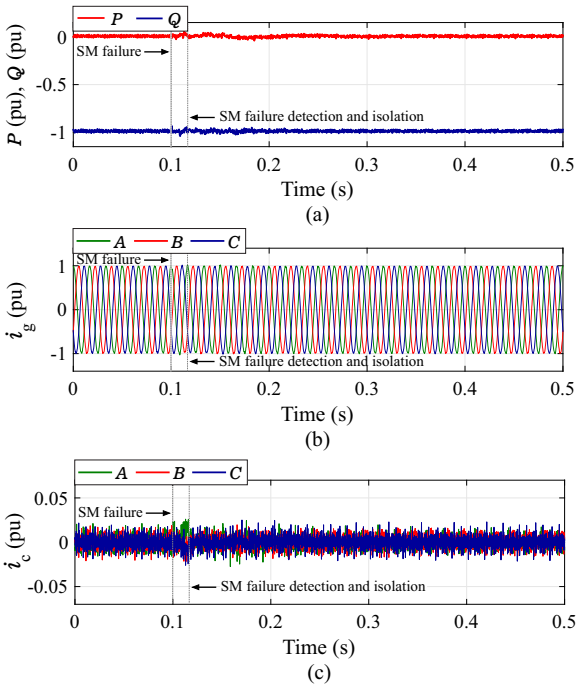
The instantaneous active and reactive powers are presented in Figure 55 (a). When a failure occurs, the SM reference voltage is maintained constant, and a smooth transient in the instantaneous powers is observed. Moreover, the grid and circulating currents are shown in Figs. 55 (b) and (c), respectively. The SM failure generate a smaller transient response

Figure 54 – SM capacitor voltages of the upper arm of MMC phase A considering AR method: (a) Measured voltages; (b) Observed voltages; (c) Relative errors.



Source: Elaborated by the author.

Figure 55 – Dynamic behavior of HB-MMC considering AR method: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents.



Source: Elaborated by the author.

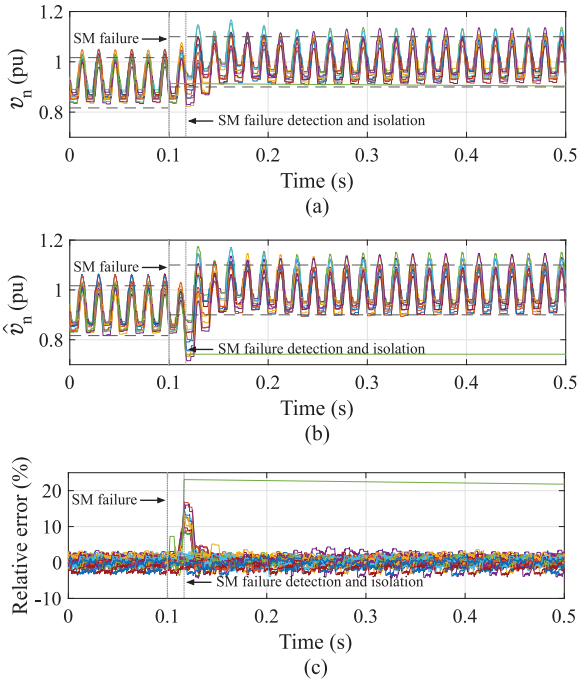
in the current dynamics, which is extinguished after approximately 10 ms. Moreover, the circulating currents reach around 0.028 pu during transient operation.

4.4.1.3 MMC Dynamics Considering Active Redundancy with Load-Sharing

Measurements and estimates of the SM capacitor voltages in pu are shown in Figs. 56 (a) and (b), respectively. As noted, the SMs operate with reduced voltage under normal conditions. The average voltage is around 0.92 pu, resulting in the utilization factor of f_{us} = 46.3%. When a failure occurs, the capacitor voltages of the remaining SMs are increased by the gain $\frac{N_T}{N_T - N_F}$, to compensate the faulty SMs in each arm. Therefore, the effective dc-link voltage is maintained at the nominal value and overmodulation region is avoided. Similar behavior is noticed in the CVI method. Moreover, the average measured voltage is around 1 pu in steady-state, leading to an utilization factor of $f_{us,f} = 50\%$. Considering the remaining SMs, the relative errors between the measured and estimated values are within $\pm$ 5% during steady-state operation, as shown in Fig. 56 (c).

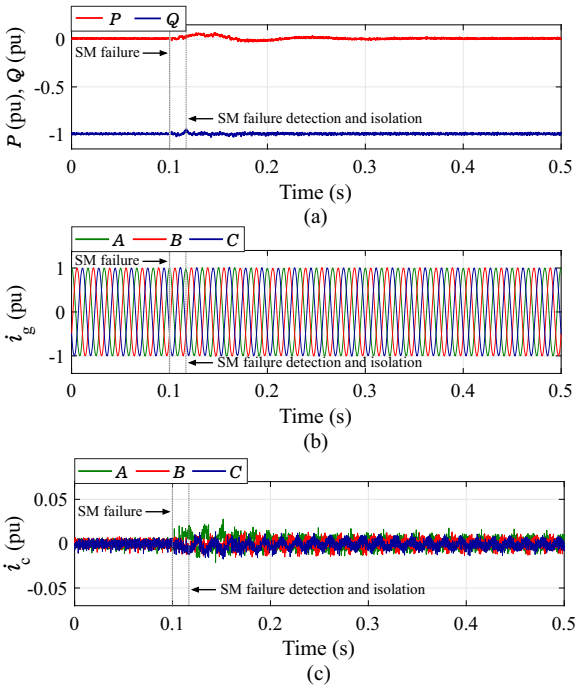
Figure 57 (a) shown the instantaneous active and reactive powers. Since the remaining SM capacitors must be charged during SM failures, similar dynamic behavior of the CVI method is noticed for the ALR method. Furthermore, the grid and circulating

Figure 56 – SM capacitor voltages of the upper arm of MMC phase A considering ALR method: (a) Measured voltages; (b) Observed voltages; (c) Relative errors.



Source: Elaborated by the author.

Figure 57 – Dynamic behavior of HB-MMC considering ALR method: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents.



Source: Elaborated by the author.

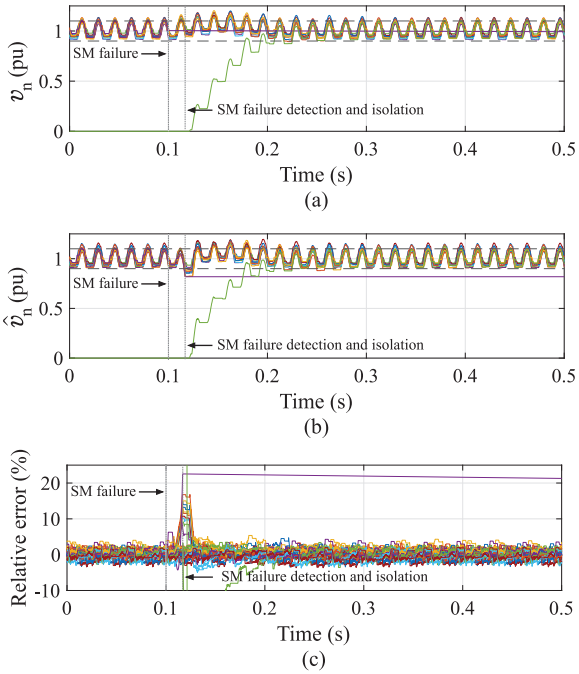
currents are shown in Figs. 57 (b) and (c), respectively. When a failure occurs, a transient response in the currents dynamics is noted, and the steady-state operation is reached after approximately 80 ms. Furthermore, the circulating currents reach around 0.03 pu during transient operation.

4.4.1.4 MMC Dynamics Considering Standby Redundancy

Measurements and estimates of the SM capacitor voltages in pu are shown in Figs. 58 (a) and (b), respectively. As noted, the non-redundant SMs are in nominal operation with average voltage value of 1 pu. Moreover, the spare SM is initially discharged and isolated from the main circuit by the bypass structure. Since the faulty SM is detected and isolated, the spare SM is inserted. During the charging process, the SM voltages reach 1.18 pu. It is important to observe that in SR strategy, the number of carriers is not changed, since the failed and spare SMs are exchanged. Furthermore, the relative errors between the measured and estimated values are illustrated in Fig. 58 (c). As noted, except for the faulty SM, the relative errors are within ± 5% during steady-state operation.

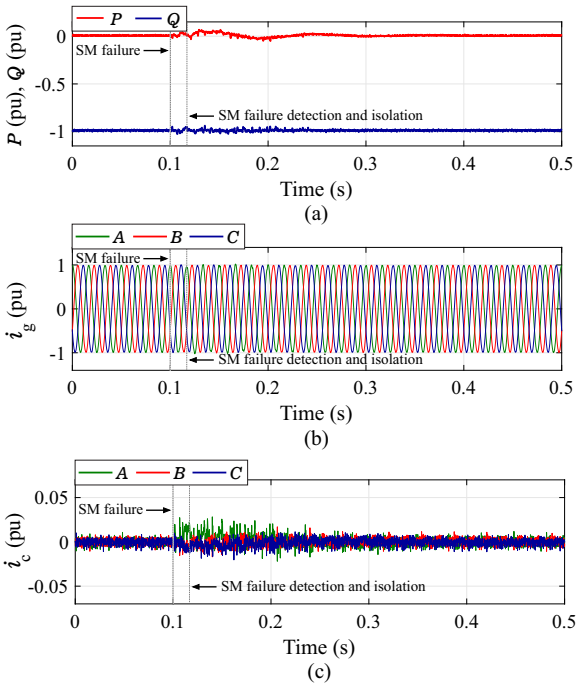
Figure 59 (a) shown the instantaneous active and reactive powers. As noted, a transient is caused by the charging process of the spare SMs, which absorbs active power

Figure 58 – SM capacitor voltages of the upper arm of MMC phase A considering SR method: (a) Measured voltages; (b) Observed voltages; (c) Relative errors.



Source: Elaborated by the author.

Figure 59 – Dynamic behavior of HB-MMC considering SR method: (a) Instantaneous active and reactive powers; (b) Grid currents; (c) Circulating currents.



Source: Elaborated by the author.

from the grid. Moreover, the grid and circulating currents are shown in Figs. 59 (b) and (c), respectively. When a failure occurs, a transient response in the currents dynamics is noted, and the steady-state operation is reached after approximately 130 ms. Furthermore, the circulating currents reach around 0.03 pu during transient operation.

4.4.2 Experimental Results

To verify the validity of both theoretical and simulation analyses, experimental results were obtained for a low-voltage MMC prototype considering the same parameters from Table 7 and the same circuit from Fig. 31. In addition, the SM capacitor voltage measurements are again considered in this study. Aiming to emulate an SM faulty during the MMC operation, 1 SM is bypassed in both upper and lower MMC arms, which S_1 is permanently turned on by $q = 0$. Under such conditions, the detection and isolation of the faulty SM is neglected. Moreover, only CVI strategy is adopted in this case. Therefore, all the 3 remaining SMs should increase the capacitor voltage to compensate the removed SM, as discussed in Section 4.3.

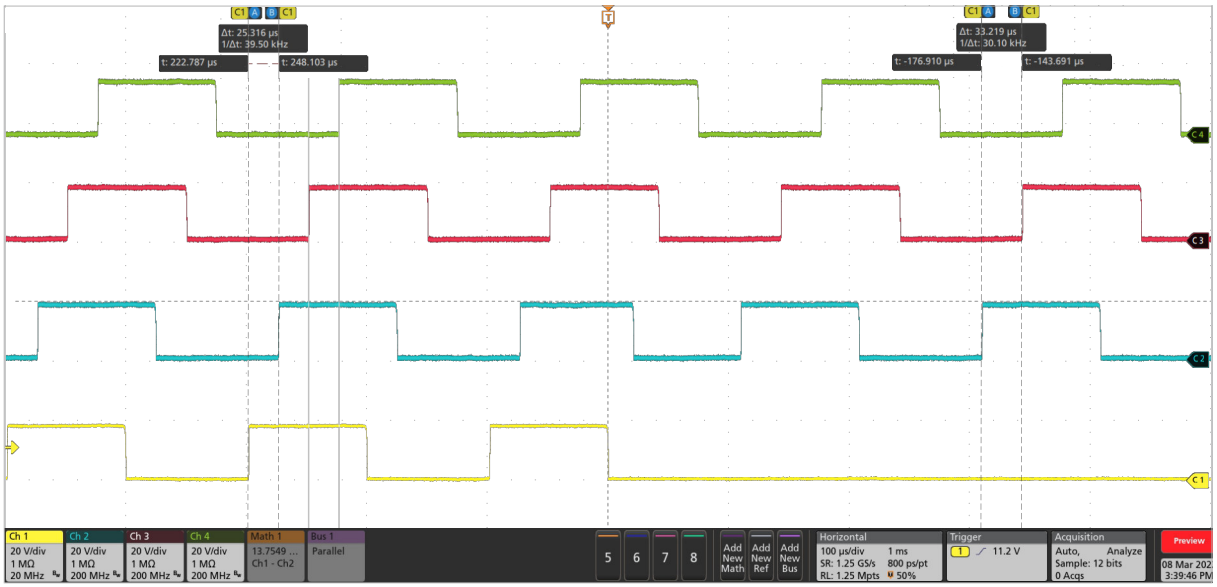
The removal of one SM is done by adapting the PS-PWM to the new configuration,

with only 3 SMs per arm, according to (4.11). As shown in Fig. 60, a phase shift of 25 μs among the carriers is observed when all the 4 SMs are operating. Moreover, when only 3 SMs are operating, the phase shift between carriers is set to 33.33 μs.

Figure 61 presents the dynamic behavior for the single-phase MMC when 1 SM is removed in each arm. As observed, all the 3 remaining SMs increase the capacitor voltage in 33%, from 100 V to 133V, to compensate the removed one. It is important to remark that such increment is to high and can bring issues to the MMC operation, for instance, due to the overvoltage protection trip in the remaining SM. Such issues are neglected at this time, since a low-voltage operation is adopted in the prototype, maintaining the voltage and current levels in the SMs far from nominal values. However, the transient in both arm and output currents is severe, reaching a peak value of around 2 pu and lasting for about 300 ms. Moreover, only 4 levels can be noticed in the arm voltages due to the removed SM.

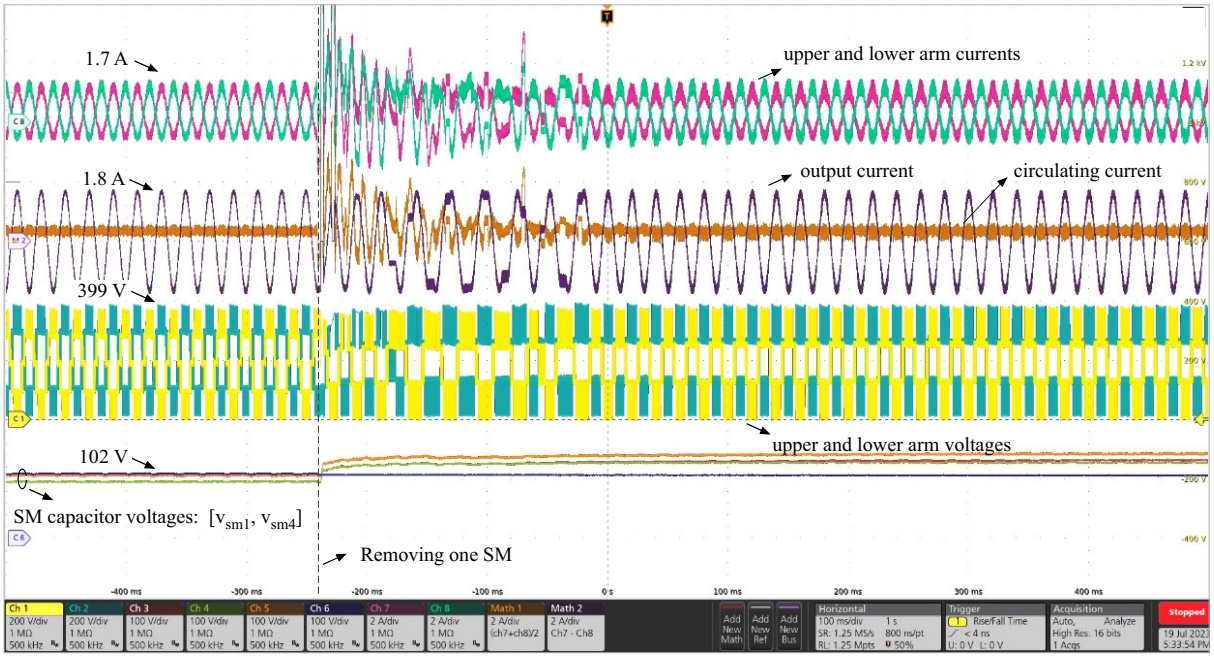
The dynamic behavior when 1 SM is inserted again in each arm is illustrated in Fig. 62. Since a long period ($>$ 3 min) is considered for the complete discharge of the removed SM, the removed SM voltage showed in Fig. 62 is close to zero. The transient effect in both arm and output currents lasts approximately 300 ms and is similarly severe as in the previous scenario. All the 4 operating SMs are then balanced around the reference value $V^* = 100V$ by about 5s reaching similar steady-state behavior as in the pre-fault condition.

Figure 60 – Dynamic behavior of the single-phase MMC during removal of one SM.



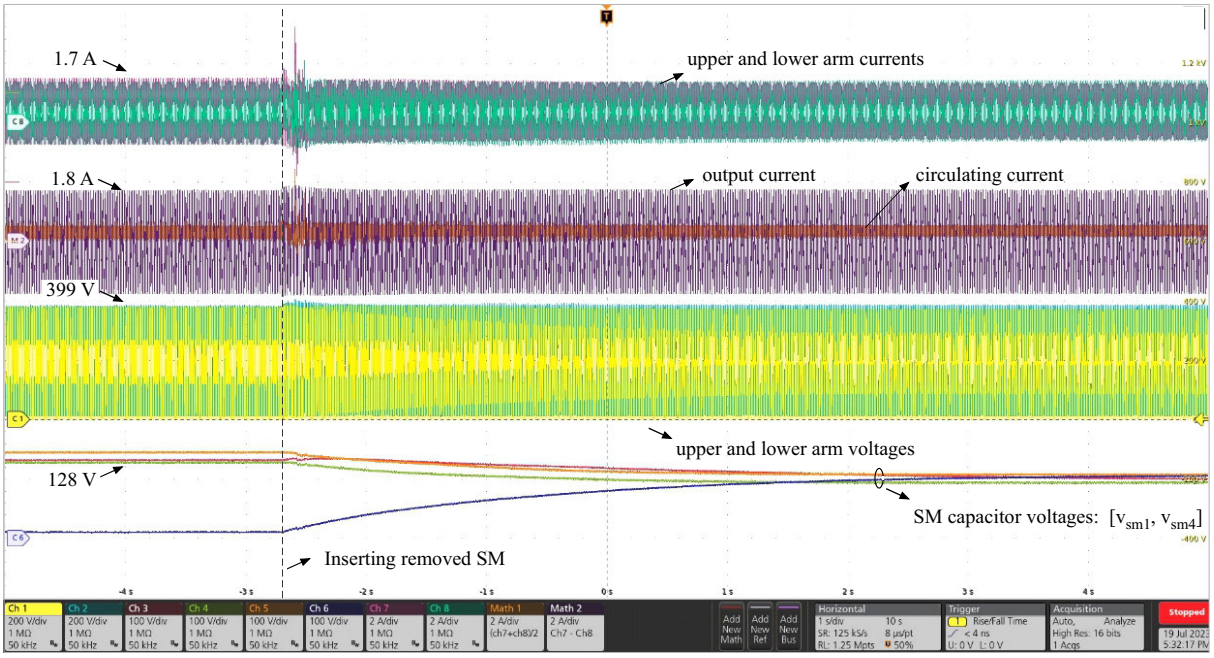
Source: Elaborated by the author.

Figure 61 – Dynamic behavior of the single-phase MMC during removal of one SM.



Source: Elaborated by the author.

Figure 62 – Dynamic behavior of the single-phase MMC during insertion of one SM.



Source: Elaborated by the author.

4.5 Conclusions

This chapter presented the main converter fault-tolerance schemes for MMC-based STATCOM systems, based on the available technical literature. Analytical expressions to determine the maximum number of SM failures in the MMC-based STATCOM systems

were employed. Thereafter, the limitations of the main converter fault-tolerance schemes under SM failures were described and critically compared. The effect of the faulty SMs on the converter dynamics for different fault-tolerance strategies were evaluated, considering the sliding-mode observer. Even considering a long detection and isolation time for the faulty SM, the observer presented suitable performance. Furthermore, experimental results validate the control strategy for CVI method in a downscaled MMC prototype.

The AR strategy presents the best performance in terms of dynamic behavior. Furthermore, the SR strategy results in the worst performance for dynamic behavior, since the charging process of the spare SMs affects the remaining SMs. The ALR and CVI strategy present similar dynamic behavior results. Additionally, CVI strategy increases the voltage stresses in the semiconductor devices, which limits the fault-tolerance capability.

The redundant SMs increase the converter reliability at the cost of increased CAPEX, OPEX and control complexity. Therefore, the next Chapter presents a methodology to provide a trade-off between cost and reliability of some MMC solutions. Such solutions are based on four fault-tolerance methods and four semiconductor blocking voltages. These designs present different number of components, cost and reliability, which are evaluated in the next Chapter.

5 Reliability-Oriented Design Based on Fault Tolerance

This chapter proposes a reliability-oriented design methodology for MMC-based STATCOM. The proposed methodology allows the design engineer to select the most suitable MMC solution according to the trade-off between the converter cost and the reliability requirement. The presented solutions are based on four fault-tolerance methods and four commercially available semiconductor blocking voltages. Moreover, the effect on MMC reliability considering the sliding-mode observer is evaluated.

5.1 Basics of Reliability Modeling

Power electronic systems play an increasingly important role in providing high efficiency power conversion. However, they are often presented with demanding operating environments that challenge their reliability (Baker et al., 2014). Depending on the application of a specific system, a number of stressors (e.g., high temperatures, temperature cycling, humidity, dust, vibration, electromagnetic interference (EMI), and radiation) can remove the component from safe operation zone. The large number of fragile elements in power electronics systems include semiconductors, capacitors, magnetics, controllers, sensors, and auxiliary devices. The failure of a single part can cause downtime and maintenance cost. The need for dependable systems forces both academia and industry to pursue advances in reliability research (Wang et al., 2014).

In general definition, reliability is the probability that a device will perform its intended working for a specified period of time under normal operation (Richardeau; Pham, 2013; IEEE, 2009). There are many reasons that can lead a device to failure. Since the risk of failures cannot be fully eliminated, they should be reduced to tolerable levels (Ferreira; Filho; Rocha, 2017). Some reasons that can lead to device failure are:

- *error*: installation errors, inappropriate use or maintenance are examples of failures caused by errors.
- *overstress*: is related to a single phenomenon (e.g., overvoltage or overload), when product capacities are exceeded.
- *wear-out*: is related to cumulative damage and aging process of the devices.
- *inherent design features*: the potential for failure is related with the project complexity.

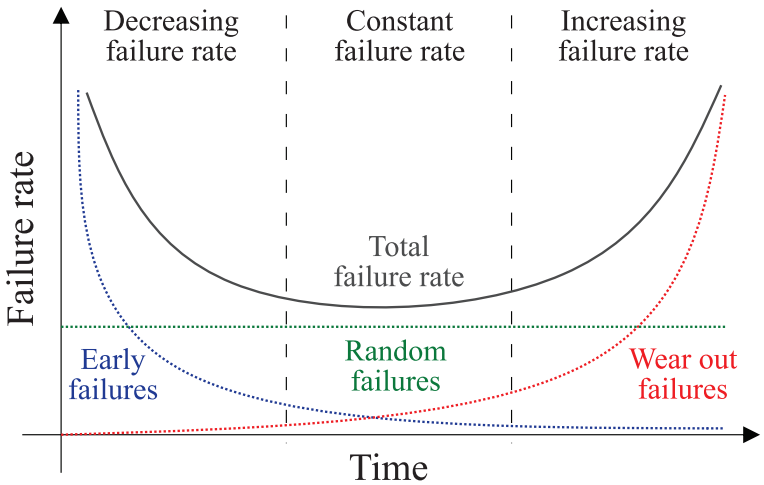
In recent years, the energy and industry segments have brought high reliability requirements for power electronic converters. In such application fields, the cost of a single failure can result in considerable financial losses. Furthermore, the critical industrial applications and harsh environmental conditions are important factors which drive studies regarding reliability in power electronic systems (Wang; Liserre; Blaabjerg, 2013).

The traditional reliability analysis of power electronic converters is based on empirical failure analysis related with historical data. Recently, the reliability engineering is going to the Physics-of-Failure approach (PoF), which is based on the mission profiles, type of failure mechanism and the related statistical model. Aiming to improve the reliability of power electronics product, a failure rate curve (also called bathtub curve) is analyzed, as shown in Fig. 63. The device failure rate is usually characterized by three regions: decreasing failure rate, constant failure rate and increasing failure rate.

The first region is mainly defined by the early failures due to manufacturing constraints. Under such conditions, burn-in testing is an important reliability technique that can be used to improve the population of a product before shipping (Vollertsen, 1999). It usually requires the electrical testing of a product, using an expected operating electrical cycle (extreme of operating condition), eliminating units that would have failed at the start of the operation. It is important to remark that the burn-in tests are carried out at the component level before being put into operation in the converter. Therefore, this region of failure can be disregarded when analyzing the MMC reliability.

The period where a constant device failure rate occurs is often referred to as the useful life of the device, which may be appropriate (although approximate) especially in electronic products. This assumption is the basis for methods to estimate system failure rates from consideration of the types and quantities of components used, such as MIL-STD-217 (Department of Defense - USA, 1991) and the Bellcore/Telcordia Technical

Figure 63 – Typical failure rate curve - bathtub curve.



Source: Adapted from Richardeau and Pham (2013).

Reference TR-332 (Bellcore, 1997). However, such databases and techniques assume that the design is perfect, the stresses are all known, everything is operated within its ratings and any single failure will cause complete device failure. Moreover, since these databases are from before the 2000s, the search for more current data extracted from the field of application is often required.

The lifetime of the device is close to its end once it enters in wear-out period (also called aging failure period), unless there is preventive maintenance or a major derating of the operation (Richardeau; Pham, 2013). Some works propose the condition monitoring in real-time process, which monitors the operation and characteristics of systems to predict upcoming fault (Han; Song, 2003). Other works propose the DfR approach as a solution to ensure a target lifetime for the power converters (Blaabjerg et al., 2017). In this concept, the design is accomplished to avoid the system to move forward to the wear-out zone. As a result, the probability of wear-out failures can be reduced during the design phase. Moreover, preventive maintenance and replacement scheduling should occur more often during the wear-out period (Tu; Yang; Wang, 2019).

Although the wear-out failures can be predicted (to some extent) and even avoided, the catastrophic/random failures are more difficult to predict (Iannuzzo, 2016). Indeed, for many electronic components, wear-out is not a practical failure mode. The time that the product is in use is significantly shorter than the operating time it takes to reach wear-out failures (Inc., 2013). Moreover, early failures are usually dealt with before shipping the product. Therefore, the reliability modeling of the MMC-based STATCOM considering only the random failures is described in the next sections.

Two important tools for reliability modeling are the reliability function $R(t)$ and failure rate $\lambda(t)$. $R(t)$ is defined as the probability that a device will perform its intended work for a specified period of time under normal operation where the device works within its safe operating area (Richardeau; Pham, 2013). $R(t)$ is given by (Todinov, 2007):

$$R(t) = \frac{N_d(t)}{N_d(0)}, \tag{5.1}$$

where $N_d(t)$ is the number of surviving devices at time t and $N_d(0)$ is the number of devices at the initial time.

The failure rate function denoted by $\lambda(t)$ is defined as the probability that a device will fail in the next time unit given that it has been working properly up to time t, i.e. (Todinov, 2007):

$$\lambda(t) = \lim \frac{N(t) - N(t + \Delta t)}{N(0)\Delta t}. \tag{5.2}$$

The relation between the failure rate $\lambda(t)$ and $R(t)$ is given by (Richardeau; Pham,

2013):

$$\lambda(t) = -\frac{1}{R(t)}\frac{dR(t)}{dt}. \tag{5.3}$$

In the constant failure region shown in Fig. 63, the devices have a long useful life period, which the failure rate is constant and equal to λ. Thus, considering the differential equation described through (5.3) and including a constant failure rate $\lambda(t) = \lambda$, the general device reliability law is:

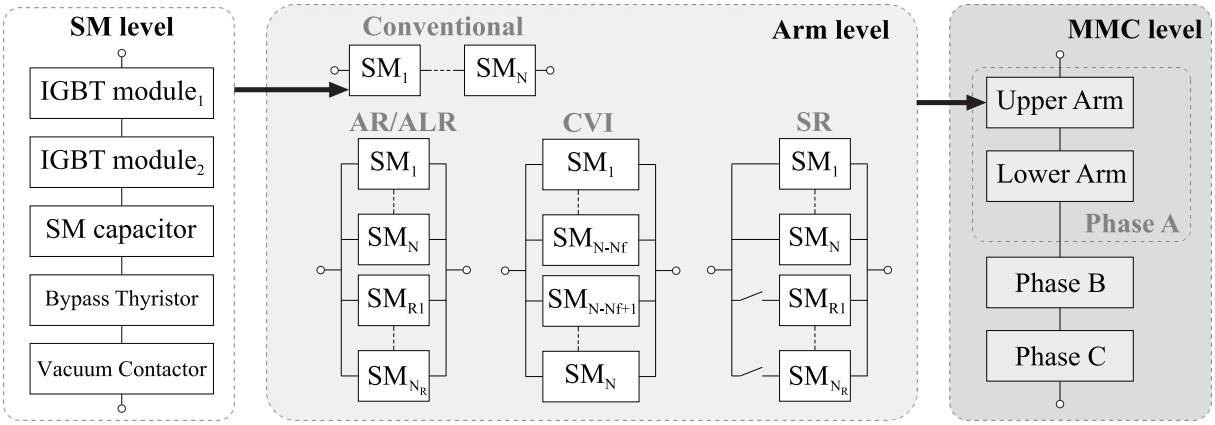
$$R(t) = e^{-\lambda t}, \tag{5.4}$$

where λ is typically expressed by failures in time (FIT), which represents one device failure in 10^9 device-operating hours.

5.2 System-Level Reliability

Since the general device reliability law is defined, the system-level reliability can be evaluated. The reliability block diagram (RBD) of the HB-MMC is subdivided into three hierarchical levels: MMC level, arm level and SM level, as observed in Fig. 64. In each hierarchical level, the RBD is used to represent the reliability relationship of MMC components (Tu; Yang; Wang, 2019). The sum of all component failure rates defines the equipment failure rate. Moreover, the sum of all failure rate assumes this is a non-fault tolerant system, meaning any single component failure would stop the system output. Hence, they are connected in series from reliability point of view. Such assumption is valid when N non-redundant SMs are employed and no fault-tolerance method is applied.

Figure 64 – Hierarchical reliability block diagram of the HB-MMC.



Source: Elaborated by the author.

The SM can operate normally only if all components are working properly. Therefore, SM-level reliability can be evaluated as a combination of the reliability of its components (Richardeau; Pham, 2013):

$$\begin{aligned} R_{SM}(t) &= R_{IGBT1}(t) \times R_{IGBT2}(t) \times R_{IGBT-GU1}(t) \times R_{IGBT-GU2}(t) \times R_{Cap}(t) \\ &\times R_{Cap-Sensor}(t) \times R_{Thy}(t) \times R_{Thy-GU}(t) \times R_{Cont}(t) \times R_{Cont-Control}(t), \end{aligned} \tag{5.5}$$

where $R_{IGBT1}(t)$, $R_{IGBT2}(t)$, $R_{IGBT-GU1}(t)$, $R_{IGBT-GU2}(t)$, $R_{Cap}(t)$, $R_{Cap-Sensor}(t)$, $R_{Thy}(t)$, $R_{Thy-GU}(t)$, $R_{Cont}(t)$, $R_{Cont-Control}(t)$ are the reliability functions of the lower IGBT power module, the upper IGBT power module, the gate unit of the lower IGBT power module, the gate unit of the upper IGBT power module, the SM capacitor, the SM capacitor voltage sensor, the bypass thyristor, the gate unit of the bypass thyristor, the vacuum contactor and the vacuum contactor control, respectively. Since the sum of all component failure rates defines the equipment failure rate, the SM-level reliability can be rewritten as:

$$R_{SM}(t) = e^{-\lambda_{SM} t}, \tag{5.6}$$

where λ_{SM} is the constant SM failure rate given by the sum of their aforementioned components, described as:

$$\begin{aligned} \lambda_{SM} &= \lambda_{IGBT1} + \lambda_{IGBT2} + \lambda_{IGBT-GU1} + \lambda_{IGBT-GU2} + \lambda_{Cap} + \lambda_{Cap-Sensor} \\ &+ \lambda_{Thy} + \lambda_{Thy-GU} + \lambda_{Cont} + \lambda_{Cont-Control}. \end{aligned} \tag{5.7}$$

Regarding the arm-level reliability, the failure rate of arm inductor is generally negligible when compared with the SM components (Guo et al., 2018b), and the arm-level reliability can be defined by the product of the reliability functions of N SMs. Assuming that each SM is independent and identical, the arm-level reliability function can be evaluated as follows (Wang et al., 2017):

$$R_{arm}(t) = \prod_{l=1}^{N} R_{SM(l)}(t). \tag{5.8}$$

Finally, the three-phase HB-MMC presents six arms in the structure. Assuming other MMC-level components are neglected and each arm is independent and identical, the MMC system-level reliability considering fault-tolerance methods can be evaluated by:

$$R_{MMC}(t) = \prod_{l=1}^{6} R_{arm(l)}(t). \tag{5.9}$$

5.3 System-Level Reliability and Fault-Tolerance Methods

The MMC arm-level reliability function can be evaluated by (5.8), only when no fault-tolerance methods are employed. However, the arm-level RBD is changed according to the applied fault-tolerance method, as illustrated in Fig. 64.

5.3.1 SM-Level Reliability Based on Fault-Tolerance Methods

Firstly, it is important to remark that the presented fault-tolerance methods are applied at SM level. Under such conditions, the failure rates of the devices can differ according to the fault-tolerance method. Regarding the ALR, all SMs share the dc-side voltage, and each of them is subjected to a lower voltage than the nominal value influencing on the reliability of IGBT modules and SM capacitors. Moreover, their failure rates are exponentially proportional to the voltage stress, described as:

$$\lambda_{b^*} = \lambda_b v_r^{\eta}, \tag{5.10}$$

where λ_b is the base failure rate and v_r is the ratio of the applied voltage to the nominal voltage. Moreover, the voltage stress factors (η) for IGBT modules are assumed as 2.43, while the value of 7.5 is chosen for capacitors, as described in (Guo et al., 2018b). Moreover, the failure rate of an SM upon j SM failures is calculated by:

$$\begin{aligned} \lambda_{SM,A_j} &= \lambda_{IGBT1_{A_j}} + \lambda_{IGBT2_{A_j}} + \lambda_{IGBT-GU1} + \lambda_{IGBT-GU2} + \lambda_{Cap_{A_j}} + \lambda_{Cap-Sensor} \\ &+ \lambda_{Thy} + \lambda_{Thy-GU} + \lambda_{Cont} + \lambda_{Cont-Control}. \end{aligned} \tag{5.11}$$

where $\lambda_{IGBT1_{A_j}}$, $\lambda_{IGBT2_{A_j}}$ and $\lambda_{Cap_{A_j}}$ are failure rates of the lower IGBT module, the upper IGBT module and the SM capacitor for j SM failures, respectively, according to (5.10).

Similar behavior is observed for the CVI method. Under such conditions, the failure rate of an SM upon j SM failures is defined as

$$\begin{aligned} \lambda_{SM,C_j} &= \lambda_{IGBT1_{C_j}} + \lambda_{IGBT2_{C_j}} + \lambda_{IGBT-GU1} + \lambda_{IGBT-GU2} + \lambda_{Cap_{C_j}} + \lambda_{Cap-Sensor} \\ &+ \lambda_{Thy} + \lambda_{Thy-GU} + \lambda_{Cont} + \lambda_{Cont-Control}. \end{aligned} \tag{5.12}$$

where $\lambda_{IGBT1_{C_j}}$, $\lambda_{IGBT2_{C_j}}$ and $\lambda_{Cap_{C_j}}$ are failure rates of the lower IGBT module, the upper IGBT module and the SM capacitor for j SM failures, respectively. Since the SMs operate under nominal voltage during normal operation, λ_{SM,C_j} differs from λ_{SM,A_j} due to the difference of v_r applied to (5.10).

Regarding the SR scheme, the standby redundant SMs are bypassed during normal operation, which are unable to enter into operation if the vacuum contactor and its control fail. Moreover, the failure rates of the standby redundant SMs are expected to be much less than that of operating SMs (Guo et al., 2018b). Under such conditions, the failure rate of the standby redundant SMs can be described by:

$$\lambda_{SM,S} = \alpha_d \lambda_{SM} + \lambda_{Cont} + \lambda_{Cont-Control}, \tag{5.13}$$

where the decrease factor $\alpha_d = 0.01$ is typically employed (Guo et al., 2018b).

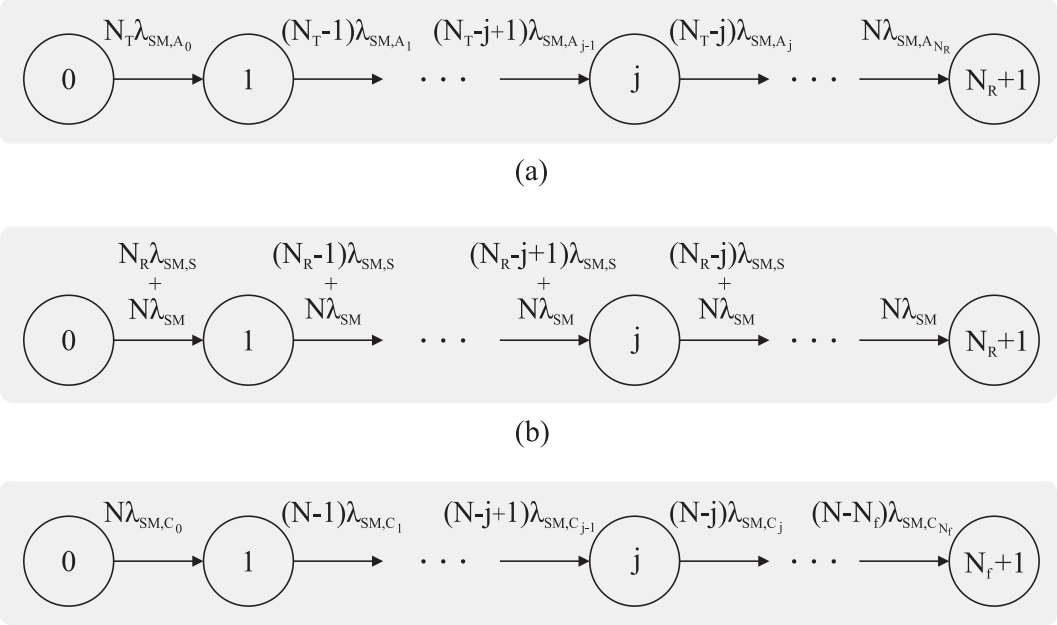
Since the SMs in the AR method present the nominal voltage during all MMC operation, the failure rates are obtained as in (5.7).

5.3.2 Arm-Level Reliability of Fault-Tolerance Methods

Aiming to evaluate the arm-level reliability considering a fault-tolerance scheme, a Markov chain model is employed (Xie et al., 2021). A conventional finite-state Markov chain is a stochastic process that satisfies the central Markov property: the present, past and future are independent. Such Markov property is a form of memorylessness, which leads to the exponential distribution (Dobrow, 2016). Therefore, since the characteristics of exponential distributions is observed considering constant failure rate, the arm-level reliability for different fault-tolerance schemes is derived in this work, based on Markov chains and the iteration method.

Regarding the redundancy strategies, when a failure of non-redundant SM occurs, the system continues to operate until the number of failures exceeds the number of redundant SMs N_R. It is noteworthy that the failure can occur in a redundant SM, since there is no difference between the redundant SMs and non-redundant SMs structure. Assuming the ALR method, the system behavior can be modeled by a Markov chain shown in Fig. 65 (a). State 0 is the initial state where all SMs are working properly. State (N_R+1) is the failed state, where the MMC is unable to operate. State j $(j = 0, ..., N_R)$ represents the system state when j SMs have failed and $(N_T - j)$ SMs are remaining. Based on the Markov chain, a set of differential equations is obtained:

Figure 65 – Markov chain for an MMC arm considering: (a) ALR method; (b) SR method; (c) CVI method.



Source: Elaborated by the author.

$$\frac{dP_{A_0}(t)}{dt} = -N_T\lambda_{SM,A_0}P_{A_0}(t),$$
$$\vdots$$
$$\frac{dP_{A_j}(t)}{dt} = (N_T - j + 1)\lambda_{SM,A_{j-1}}P_{A_{j-1}}(t) - (N - j)\lambda_{SM,A_j}P_{A_j}(t),$$
$$\vdots$$
$$\frac{dP_{A_{(N_R+1)}}(t)}{dt} = N\lambda_{SM,A_{N_R}}P_{A_{N_R}}(t), \tag{5.14}$$

where $P_{A_j}(t)$ is the probability of the MMC arm in state j considering the ALR method. Applying Laplace transforms in the equations above and inverse Laplace transforms, the differential equations are solved as follows:

$$P_{A_0}(t) = e^{-N_T\lambda_{SM,A_0}t},$$
$$\vdots$$
$$P_{A_j}(t) = \int_0^t (N_T - j + 1)\lambda_{SM,A_{j-1}}e^{-(N_T-j)\lambda_{SM,A_j}\tau}P_{Aj-1}(t-\tau)d\tau,$$
$$\vdots$$
$$P_{A_{(N_R+1)}}(t) = \int_0^t N\lambda_{SM,A_{N_R}}P_{A_{N_R}}(\tau)d\tau. \tag{5.15}$$

Moreover, the probabilities of the arm in all states can be solved iteratively. The reliability function of the arm is calculated as the sum of the probabilities of all success states (state $0 \rightarrow N_R$), given by:

$$R_{arm,ALR}(t) = \sum_{j=0}^{N_R} P_{A_j}(t). \tag{5.16}$$

It is important to remark that the arm-level reliability for AR method is a special case of (5.14-5.16). In this case, all SMs operate under nominal voltage during the whole MMC operation. Therefore, (5.8) can be represented by *N-out-of-*N_T system, where N_T-component system works if and only if at least N components in the system are in a good state (Way; Zuo, 2003). Under such conditions, the MMC arm-level reliability can be evaluated through the sum of the probability of more than N SMs inside a set of N_T are in good condition, given by (Tu; Yang; Wang, 2019):

$$R_{arm,AR}(t) = \sum_{i=N}^{N_T} C_{N_T}^{i} R_{SM}(t)^i (1 - R_{SM}(t))^{N_T - i}. \tag{5.17}$$

where $C_{N_T}^{i}$ is the number of combinations in a group of i devices inserted into a set of N_T.

When SR method is considered, a similar approach is employed based on the Markov chain of Fig. 65 (b). Thus, a set of differential equations is obtained:

$$\begin{aligned}
\frac{dP_{S_0}(t)}{dt} &= -(N_R\lambda_{SM,S} + N\lambda_{SM})P_{S_0}(t), \\
&\vdots \\
\frac{dP_{S_j}(t)}{dt} &= \left[(N_R - j + 1)\lambda_{SM,S} + N\lambda_{SM}\right] P_{S_{j-1}}(t) - \left[(N_R - j)\lambda_{SM,S} + N\lambda_{SM})\right] P_{S_j}(t), \\
&\vdots \\
\frac{dP_{S_{(N_R+1)}}(t)}{dt} &= N\lambda_{SM} P_{S_{N_R}}(t),
\end{aligned} \tag{5.18}$$

where $P_{S_j}(t)$ is the probability of the MMC arm in state j considering the SR method. Moreover, the differential equations are given by:

$$
\begin{aligned}
P_{S_0}(t) &= e^{-(N_R\lambda_{SM,S}+N\lambda_{SM})t}, \\
&\vdots \\
P_{S_j}(t) &= [(N_R-j+1)\lambda_{SM,S}+N\lambda_{SM}]\int_0^t e^{\left[(N_R-j)\lambda_{SM,S}+N\lambda_{SM}\right]\tau}P_{S_{j-1}}(t-\tau)d\tau, \\
&\vdots \\
P_{S_{(N_R+1)}}(t) &= \int_0^t N\lambda_{SM}P_{S_{N_R}}(\tau)d\tau.
\end{aligned} \tag{5.19}
$$

Therefore, the reliability function of the arm considering SR method is given the sum of the probabilities of all success states (state $0 \rightarrow N_R$):

$$
R_{arm,SR}(t) = \sum_{j=0}^{N_R} P_{S_j}(t). \tag{5.20}
$$

Regarding the CVI method, only N non-redundant SMs are employed. Under such conditions, the uninterrupted operation of the MMC is defined by N_f, which is the number of failures allowed by CVI method, as defined in 4.2. Therefore, based on the Markov chain of Fig. 65 (c), a set of differential equations is obtained:

$$
\begin{aligned}
\frac{dP_{C_0}(t)}{dt} &= -N\lambda_{SM,C_0}P_{C_0}(t), \\
&\vdots \\
\frac{dP_{C_j}(t)}{dt} &= (N-j+1)\lambda_{SM,C_{j-1}}P_{C_{j-1}}(t)-(N-j)\lambda_{SM,C_j}P_{C_j}(t), \\
&\vdots \\
\frac{dP_{C_{(N_f+1)}}(t)}{dt} &= (N-N_f)\lambda_{SM,C_{N_f}}P_{C_{N_f}}(t),
\end{aligned} \tag{5.21}
$$

where $P_{C_j}(t)$ is the probability of the MMC arm in state j. Furthermore, the differential equations can be described by:

$$
\begin{aligned}
P_{C_0}(t) &= e^{-N\lambda_{SM,C_0}t}, \\
&\vdots \\
P_{C_j}(t) &= \int_0^t (N-j+1)\lambda_{SM,C_{j-1}}e^{-(N-j)\lambda_{SM,C_j}\tau}P_{C_{j-1}}(t-\tau)d\tau, \\
&\vdots \\
P_{C_{(N_f+1)}}(t) &= \int_0^t (N-N_f)\lambda_{SM,C_{N_f}}P_{C_{N_f}}(\tau)d\tau.
\end{aligned} \tag{5.22}
$$

Thus, the reliability function of the arm considering CVI method is given the sum of the probabilities of all success states (state $0 \rightarrow N_f$):

$$R_{arm,CVI}(t) = \sum_{j=0}^{N_f} P_{C_j}(t). \tag{5.23}$$

Since the adopted method includes integrations and iterations, the probability of the system in each state is solved using the Euler method through MATLAB.

5.3.3 MMC-Level Reliability Based on Fault-Tolerance Methods

The MMC-level components such as cooling, control, and protection systems are also critical for the MMC reliability. However, aims to compare the MMC reliability under different fault-tolerance schemes, such MMC-level components are neglected to provide a simplified reliability model. Under such conditions, only the six MMC arms are considered. Therefore, assuming that each arm is independent and identical, the MMC system-level reliability can be evaluated by:

$$R_{MMC}(t) = \prod_{l=1}^{6} R_{arm,ft(l)}(t). \tag{5.24}$$

where $R_{arm,ft}$ is the arm-level reliability according to the chosen fault-tolerance method.

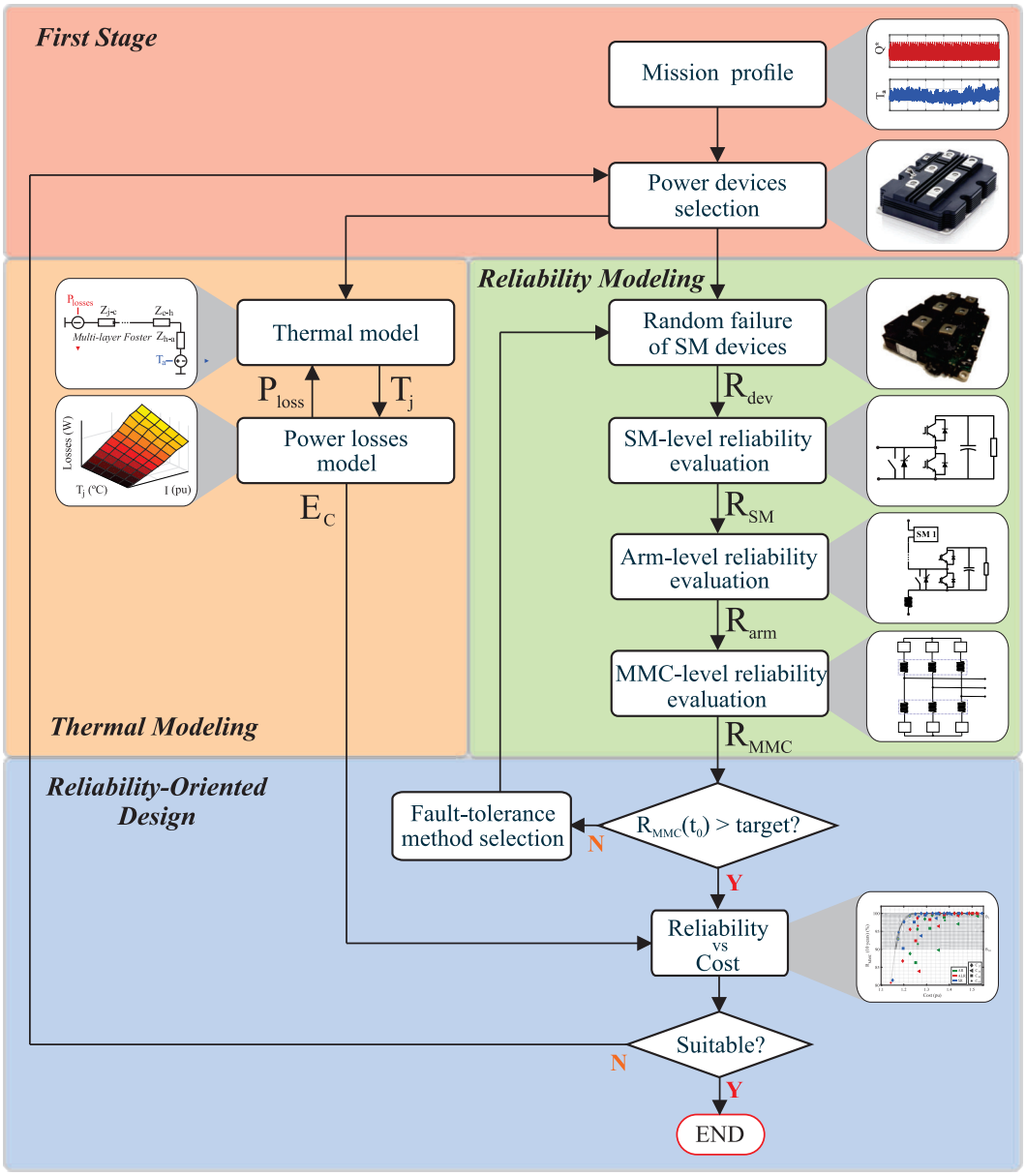
5.4 Reliability-Oriented Design Based on Fault-Tolerance Methods

From the industry point of view, the converter must be designed to achieve a reliability level $R(t_0)$ for a defined target lifetime t_0, regarding its specific application (Wang et al., 2014). Therefore, a tool that allows the design engineer to select the most suitable MMC solution according to the trade-off between the converter cost and the reliability requirement is illustrated in Fig. 66.

5.4.1 First Stage

First, the mission profile is defined for the considered application. Measurements of reactive power and ambient temperature (T_a) mission profiles are employed to define the system operating condition. The most appropriate power devices can be selected according to the power rating, voltage and current levels.

Figure 66 – Flowchart of the reliability-oriented design.



Source: Elaborated by the author.

5.4.2 Thermal Modeling

The thermal model is based in a partial-fraction circuit, also known as the Foster Model. This model is employed to estimate the junction temperature (T_j) and case temperature of each power device disregarding the cross-coupling effect between the devices, as observed in Fig. 67. The Foster model parameters are based on mathematical fitting of the measured/simulated temperature curves. Each RC parameter in the Foster network represents no physical meaning. Moreover, the junction-to-case transient thermal impedances Z_{j-c} are usually specified based on a Foster model in the datasheets. The case-to-heatsink impedance Z_{c-h} is represented by a thermal resistance.

The heatsink-to-fluid impedance Z_{h-f} presents a parallel connection of the thermal

resistance R_{h-f} and the capacitance C_{h-f}. Heatsink parameters can be estimated through the simplified methodology proposed by Asimakopoulos et al. (2015). This methodology considers an uniform temperature profile throughout the power devices baseplate solder and cooling plate. The heatsink geometry has a simple rectangular cross-section and is approximated by a simple orthogonal brick. Under such conditions, the heatsink parameters can be computed by:

$$R_{h-f} = \frac{d_h}{\kappa_h A_h}, \tag{5.25}$$

$$C_{h-f} = c_h \rho_h d_h A_h, \tag{5.26}$$

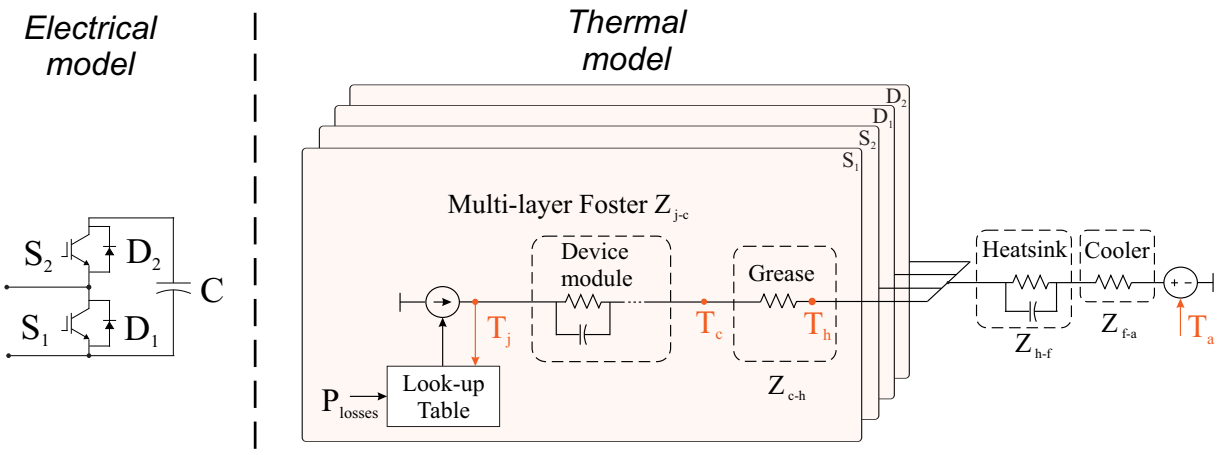
where d_h is the heatsink thickness, κ_h is the thermal conductivity of the heatsink material, A_h is the heatsink surface area, c_h is the specific heat capacity and ρ_h is the material density.

The cooling system improves the heat exchange from the heatsink to the ambient, described by Z_{f-a}. This thermal resistance presents a series connection to the heatsink and can be calculated by (Asimakopoulos et al., 2015):

$$R_{f-a} = \frac{1}{f_{fc} A_h}, \tag{5.27}$$

where f_{fc} is the fluid flow convection coefficient (Incropera; DeWitt, 1996). The power losses model employed is based on a lookup table of losses for each semiconductor device.

Figure 67 – Thermal model based on Foster model with heatsink and cooling system.



Source: Elaborated by the author.

5.4.3 Reliability Modeling

The first iteration of the algorithm considers the conventional approach, where only N non-redundant SMs and no fault-tolerance method are applied. Under such conditions, the SM-level reliability is calculated by (5.6). It is important to remark that other components can be included at the SM-level reliability, such as SM control system and power supply. Therefore, the failure rate of such components must be summed in (5.7). Moreover, the arm-level reliability can be evaluated by the product of the reliability functions of N SMs, as given in (5.8), if other arm components are neglected. Thus, the MMC system-level reliability can be calculated by (5.9) and analyzed for a given lifetime target.

As observed in Fig. 66, some fault-tolerance method must be included in the MMC design, if the given lifetime target is unreached. Therefore, the SM-level reliability is changed according to the applied fault-tolerance method, as described in Section 5.3. Furthermore, the arm-level reliability is derived using Markov chains and the iteration method. Regarding redundancy-based methods, the number of redundant SMs N_R is increased until the given converter lifetime target is reached. On the other hand, when the CVI method is employed, the MMC-level reliability is evaluated according to the number of failures allowed N_f. It is important to note that the given lifetime target can be unachieved, since the N_f is inherently limited for the CVI method. Finally, the MMC system-level reliability can be calculated by (5.24) according to the chosen fault-tolerance method.

5.4.4 Reliability-Oriented Design

The converter reliability requirement may be more stringent depending on the approach applied. For example, B_x approach is given according to the reliability-level such as:

- B_1 lifetime approach, the MMC reliability $R_{MMC}(t_0) \geq 0.99$.
- B_{10} lifetime approach, the MMC reliability $R_{MMC}(t_0) \geq 0.90$.

If the required MMC reliability is not met (e.g., $R_{MMC}(t_0) < 0.99$), some fault-tolerance method can be employed aiming to fulfill the reliability criterion (e.g., $R_{MMC}(t_0) \geq 0.99$). Therefore, the overall cost of the solution must be known, allowing the choice of the most suitable MMC solution. Typically, the figure of merit of the overall MMC cost includes the CAPEX and OPEX. The CAPEX is mainly related to investment in power electronics (e.g., semiconductor devices, controls, cabinets), which is dominant in the initial investment of the converter (Siddique et al., 2016). Thus, the cost of power electronics is based on the switching power installed as follows:

$$K_{sw} = 12 N_T K_c V_{svc} I_{svc}, \tag{5.28}$$

where I_{svc} is the rated device current. $K_c = 3.5$ €/kVA is employed (Siddique et al., 2016) in this work. Moreover, the costs of passive elements should be included. According to Fujii, Schwarzer and De Doncker (2005), the cost of the SM capacitors K_{cap} are 150 €/kJ. Furthermore, the cost of the magnetic devices K_{mag} in euros can be estimated by:

$$K_{mag} = 4000 N_{mag} + 723000 A_p, \tag{5.29}$$

where N_{mag} is the number of inductors and A_p is the total area product (in m^4) of the cores of all inductors. The area product of a single magnetic core is the product of the winding-window area and the core cross-sectional area. Finally, the capital expenditure is given by:

$$CAPEX = K_{sw} + K_{cap} + K_{mag}. \tag{5.30}$$

Regarding OPEX, the semiconductor conduction and switching losses are predominant (Tu; Yang; Wang, 2019). Under such conditions, the operational expenditure of the converter is considered as follows:

$$OPEX = K_o E_c(t_0), \tag{5.31}$$

where K_o is the price per kilowatt-hour and E_c is energy consumption of the converter. Based on loss penalty for transmission system, $K_o = 0.11$ €/kWh is employed (Alvarez et al., 2016). Thus, the overall cost is given by:

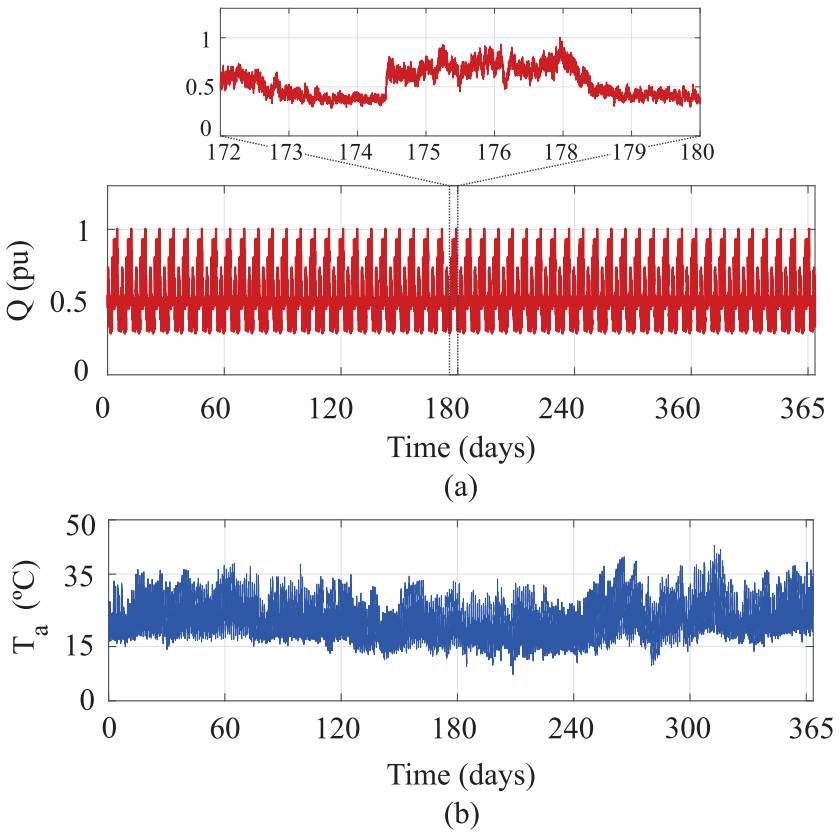
$$Cost = CAPEX + OPEX, \tag{5.32}$$

It is important to remark that the design which meets the MMC reliability criterion at the lowest cost is the most suitable.

5.5 Case Study

PLECS simulations are used to estimate the MMC power losses, while the reliability evaluation is obtained by MATLAB software. The converter is submitted to a mission profile based on a reactive power demand of a food industry in southeastern Brazil, along with ambient temperature measurements, as presented in Fig. 68. As noted, the reactive power demand profile is obtained with a sampling time of 5 minutes over a week and replicated over a year.

Figure 68 – Mission profiles with a sampling time of 5 min: (a) Reactive Power; (b) Ambient Temperature.



Source: Elaborated by the author.

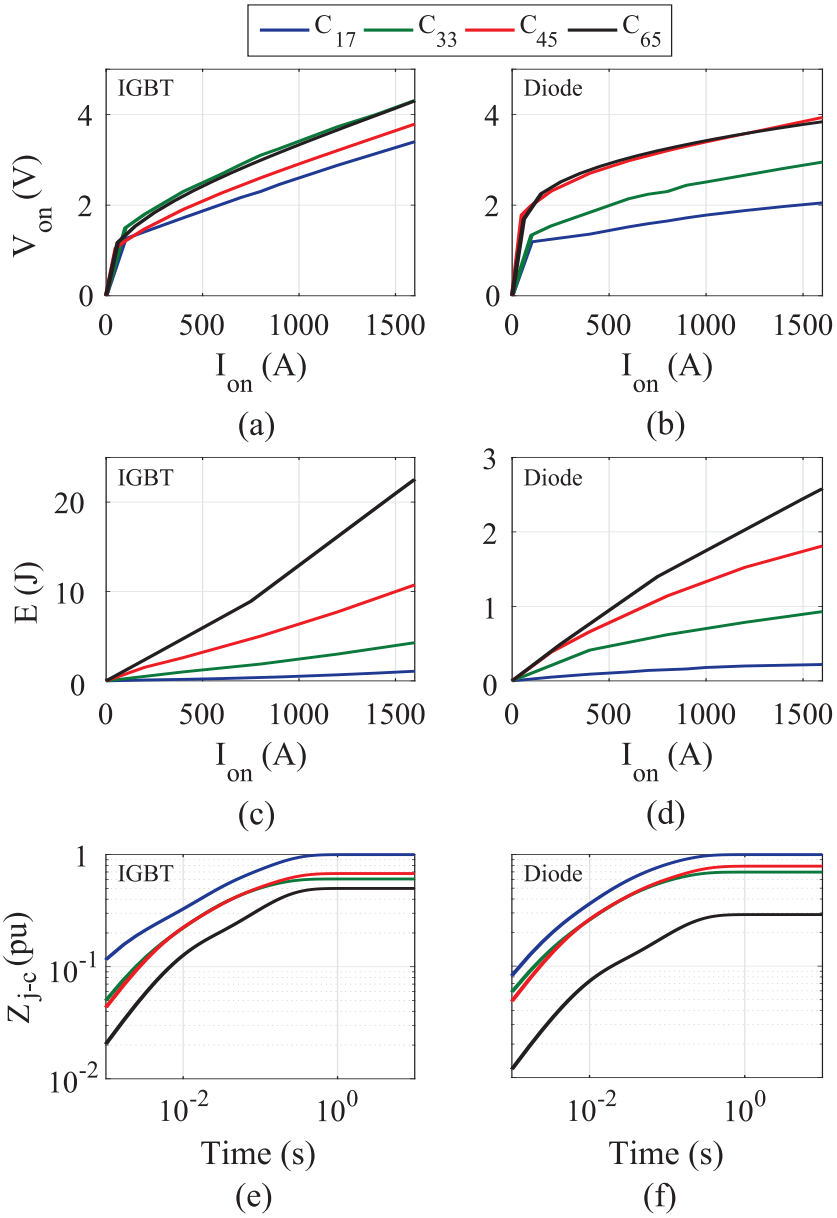
Table 11 shows the part numbers employed in the MMC designs. Four different ABB HiPak IGBTs modules with blocking voltage capability range between 1.7 kV and 6.5 kV are considered. Commercially available modules with rated current close to 800 A are selected. Moreover, the same parameters presented in Tab. 5 are employed in this chapter.

Figure 69 presents the typical HiPak power devices curves extracted from datasheets. All curves are evaluated for a junction temperature of 25°C. The IGBT and diode conduction power losses can be evaluated through the curves shown in Fig. 69 (a) and (b). Moreover, Figure 69 (c) and (d) illustrated the IGBT and diode switching losses. All utilization factors have similar values. The IGBT switching energy curves include both turn-on

Table 11 – HiPak IGBT modules specifications for four proposed solutions.

Case	Voltage (V)	Current (A)	Part Number
C_{17}	1700	800	5SND 0800M170100
C_{33}	3300	800	5SNA 0800N330100
C_{45}	4500	800	5SNA 0800J450300
C_{65}	6500	750	5SNA 0750G650300

Figure 69 – Power devices curves extracted from datasheets: (a) IGBT on-state characteristics; (b) Diode forward characteristics; (c) IGBT switching energies per pulse; (d) Diode reverse recovery characteristics; (e) IGBT transient thermal impedance ($Z_b = 0.021K/W$); (f) Diode transient thermal impedance ($Z_b = 0.036K/W$).



Source: Elaborated by the author.

and turn-off switching energies data. Moreover, the junction-to-case transient thermal impedances are usually specified based on a Foster model in the datasheets. Figures 69 (e) and (f) present the normalized transient thermal impedances for semiconductor devices. The Foster parameters extracted from datasheets were converted to Cauer parameters through software PLECS.

Regarding the heatsink parameters, the values of R_{h-f} and C_{h-f} vary according to the heatsink area and thickness. In this work, the area is considered to be equal to

Table 12 – Heatsink and cooling system parameters.

Case	R_{h-f} (K/W)	C_{h-f} (J/K)	R_{f-a} (K/W)
C_{17}	0.007	1327	0.130
C_{33}	0.007	1327	0.070
C_{45}	0.007	1327	0.050
C_{65}	0.005	1939	0.030

the total area of the power module obtained from the device datasheet. Furthermore, aluminum heatsinks with 3 cm of thickness are employed (Asimakopoulos et al., 2015). The water-cooling system are evaluated to ensure similar temperature stresses in each IGBTs module solution (Incropera; DeWitt, 1996; Farias et al., 2018). The water flow convection coefficient f_{fc} can range from 50 to 2500 $W/(m^2K)$, depending on the speed and type of water flow, temperature dependent properties, and pressure (Incropera; DeWitt, 1996). The manufacturer indicates maximum values of 150 °C and 125 °C, for the junction and case temperatures, respectively.

The water flow convection coefficient is adjusted to maintain the average heatsink temperature close to 60 °C, during 1 pu of reactive power for all cases. Table 12 presents the parameters of the heatsinks and cooling system. As observed, the resistance and capacitance parameters of the heatsink have approximate values due to the similar dimensions of the power modules. Therefore, a lower thermal resistance in the cooling system is required for the power modules that present higher losses.

All component failure rates employed in this work are presented in Table 13. The FIT rates are those commonly observed in the field (unlike those found in Military standards) (Ladoux; Serbia; Carroll, 2015), with the exception of the SM capacitor voltage sensor obtained from Julian and Oriti (2006). Moreover, the SM capacitor FIT rate is obtained from specifications of EPCOS (Corporation, 2009). It is important to remark that the FIT of the IGBT module and SM capacitor is evaluated according to the SM

Table 13 – Failure rate data of the MMC components for different MMC solutions.

Component	FIT (failures/10^9hours)				
	SM	C_{17}	C_{33}	C_{45}	C_{65}
IGBT Module	180(2)	9403	4479	4058	2472
IGBT Module Gate Unit	150(2)	8700	4500	3300	2100
SM Capacitor	300	6299	2527	3558	1978
SM Capacitor Voltage Sensor	150	4350	2250	1650	1050
Bypass Thyristor	20	580	300	220	140
Bypass Thyristor Gate Unit	100	2900	1500	1100	700
Vacuum Contactor	100	2900	1500	1100	700
Vacuum Contactor Control	100	2900	1500	1100	700
Total	1430	38032	18556	16086	9840

Table 14 – SM capacitors and magnetic devices parameters for cost design.

Parameters	MMC specifications			
	$\mathbf{C}_{17}$	$\mathbf{C}_{33}$	$\mathbf{C}_{45}$	$\mathbf{C}_{65}$
A_p ($\mathrm{m}^4 \cdot 10^{-3}$)	20.05	39.11	53.08	76.70
E_{cap} (kJ)	612	612	612	612

voltage, as described in (5.10).

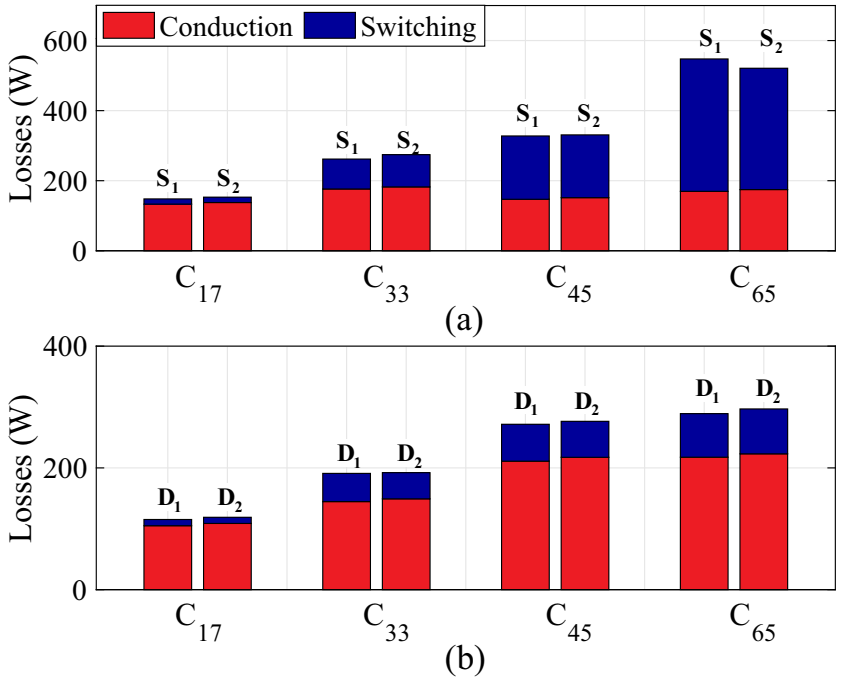
The typical lifetime target of power electronics systems, from industry perspective, is described in (Falck et al., 2018). For STATCOM applications, such as industrial and wind power systems, an expected lifetime greater than 10 years is reported (Wang et al., 2014). Therefore, a conservative MMC lifetime target is defined in this work as 10 years of operation. Finally, the energy stored in SM capacitors E_{cap} and A_p values are given in Table 14. The MMC presents $N_{mag} = 6$ and the capacitive energy stored is 36 kJ/MVA for all cases, as described in Chapter 2.

5.6 Results

5.6.1 MMC Power Losses and Reliability Assessments

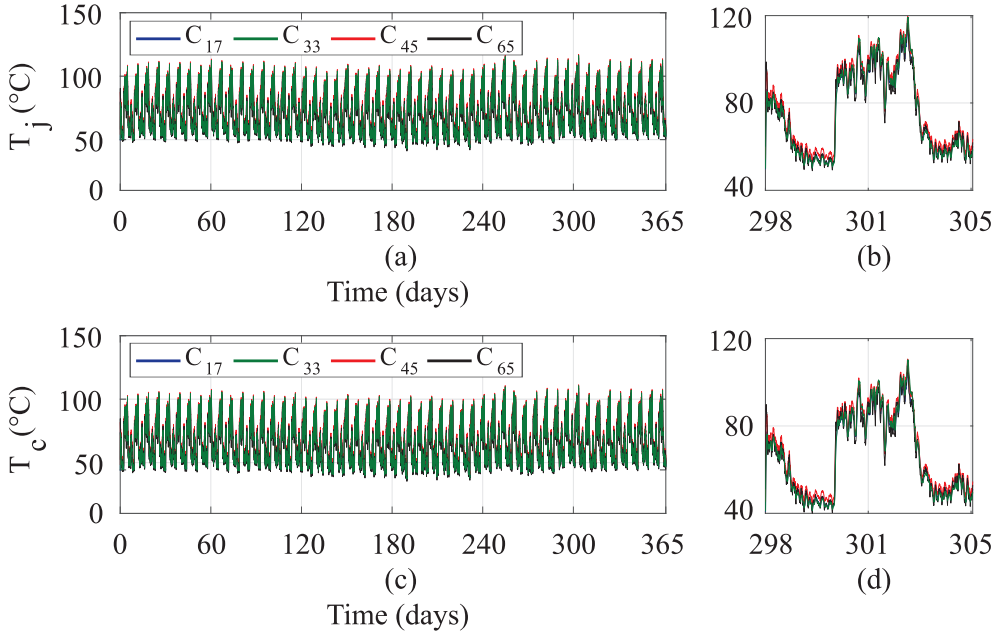
Initially, semiconductors power losses for all cases are shown in Fig. 70. All cases are evaluated for a junction temperature of 25 °C and 1.0 pu of reactive power in inductive

Figure 70 – Power losses for all cases of power devices: (a) S_1 and S_2; (b) D_1 and D_2.



Source: Elaborated by the author.

Figure 71 – Temperatures of the more stressed device D_2 in an SM for four designs: (a) Junction temperatures; (b) Detail of junction temperatures; (c) Case temperatures; (d) Detail of case temperatures.



Source: Elaborated by the author.

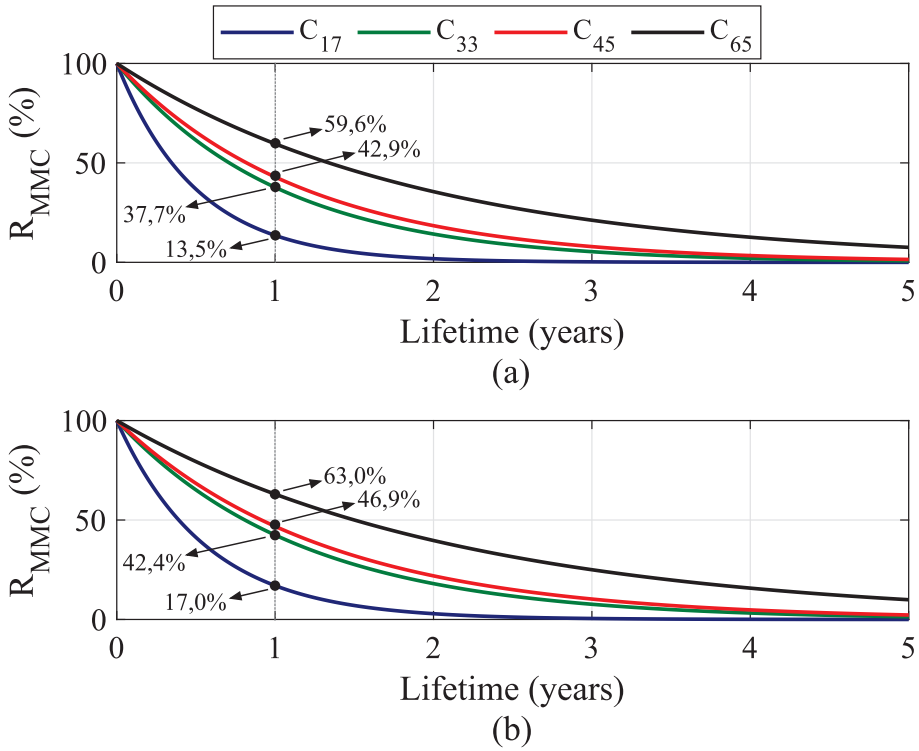
operation. As observed, an increase in the blocking voltages of power devices causes an increase in switching losses. This result is consistent with the curves extracted from datasheets shown in Fig. 69. Furthermore, diodes with higher blocking voltages present higher conduction losses, whereas this relationship is not straightforward for IGBTs. The IGBTs based on C_{33} solution present higher conduction losses. Moreover, the design based on C_{17} has the lowest total power losses in an SM.

Based on the application mission profile, the diode D_2 is the most stressed device in an SM. Under such conditions, Figure 71 presents the junction and case temperature in D_2 for all cases. As observed, the maximum junction and case temperature are approximately 120 °C and 110 °C, respectively. Moreover, all cases have similar thermal stresses.

The MMC-level reliability for the four analyzed cases are shown in Fig. 72 (a), considering the converter with SM capacitor voltage measurements. As observed, solutions with the highest number of SMs present smaller MMC-level reliability. Therefore, the random failures have more influence on the converter lifetime for designs with more SMs. The solution based on the design C_{65} presents the highest reliability, 59.6% for 1 year of operation. Furthermore, C_{17} has the lowest reliability, 13.5%.

Since the SM capacitor voltage measurements are neglected assuming the sliding-mode observer, the MMC-level reliability is improved for all solutions, as illustrated in Fig. 72 (b). Under such conditions, the solution based on the design C_{65} presents the highest reliability, 59.6% against 13.5% of the lowest reliability reach by C_{17}. It is

Figure 72 – MMC system-level reliability function for different solutions: (a) with SM capacitor voltage measurement; (b) without SM capacitor voltage measurement (sliding-mode observer).



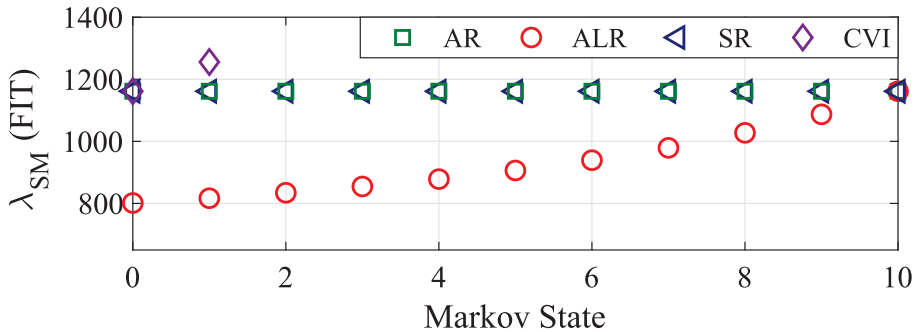
Source: Elaborated by the author.

important to remark that the converter lifetime target ($t_0 = 10$ years) is unreached for all presented solutions, considering both B_1 or B_{10} approaches.

5.6.2 MMC Redundancy Design Based on Reliability Assessment

Aiming to improve the MMC-level reliability, fault-tolerance methods are included for each MMC solution. Figure 73 shows the SM failure rate of the remaining operating SMs under SM failures. For the sake of simplicity, only solutions based on the design C_{17}

Figure 73 – Effect of faulty SMs on failure rate of remaining operating SMs.



Source: Elaborated by the author.

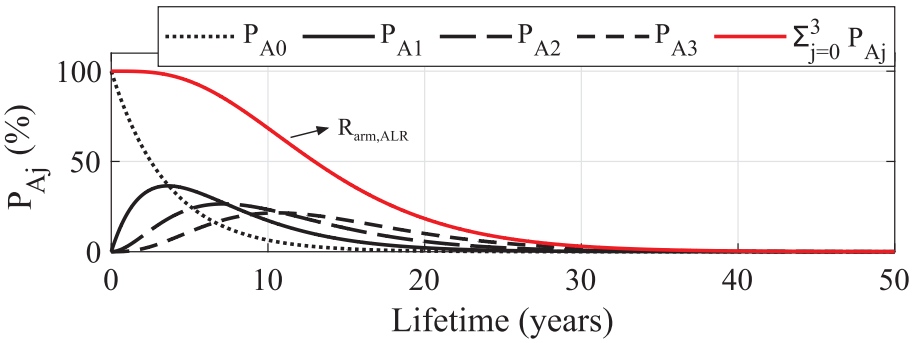
are presented, considering $N_R = 10$ SMs. The AR and SR schemes present similar SM failure rate for all Markov states (number of SM failures). The ALR method presents approximately 30% reduction in the SM failure rate, reaching the same failure rate of 1161 FIT in the failure limit operation. Moreover, the SM failure rate is increased by around 8% for the maximum number of SM failures allowed in the CVI method, since the voltage ratio is increased.

Figure 74 show the probabilities of all success states for the solution based on the design C_{17} considering the ALR method with $N_R = 3$. As noted, the reliability function of the arm is calculated as the sum of the probabilities of all success states. Under such conditions, the increase in redundant SMs causes an increase in the reliability of the MMC arm, since only SMs are considered in the reliability analysis of the MMC arm.

The effect of increasing redundant SMs on arm-level reliability for different fault-tolerant methods is evaluated based on the design C_{17} with $N_R = 3$ and $N_R = 7$, as shown in Figs. 75 (a) and (b), respectively. As noted, the CVI method has the same impact on the improvement of the arm-level reliability for both situations, since the CVI method employ only non-redundant SMs. Moreover, the CVI method is limited by the voltage ratio that can be increased until the safe limits of the MMC operation. The ALR scheme presents the highest arm-level reliability, followed by SR and AR methods, respectively. Furthermore, the arm-level reliability is improved according to the increment of redundant SMs.

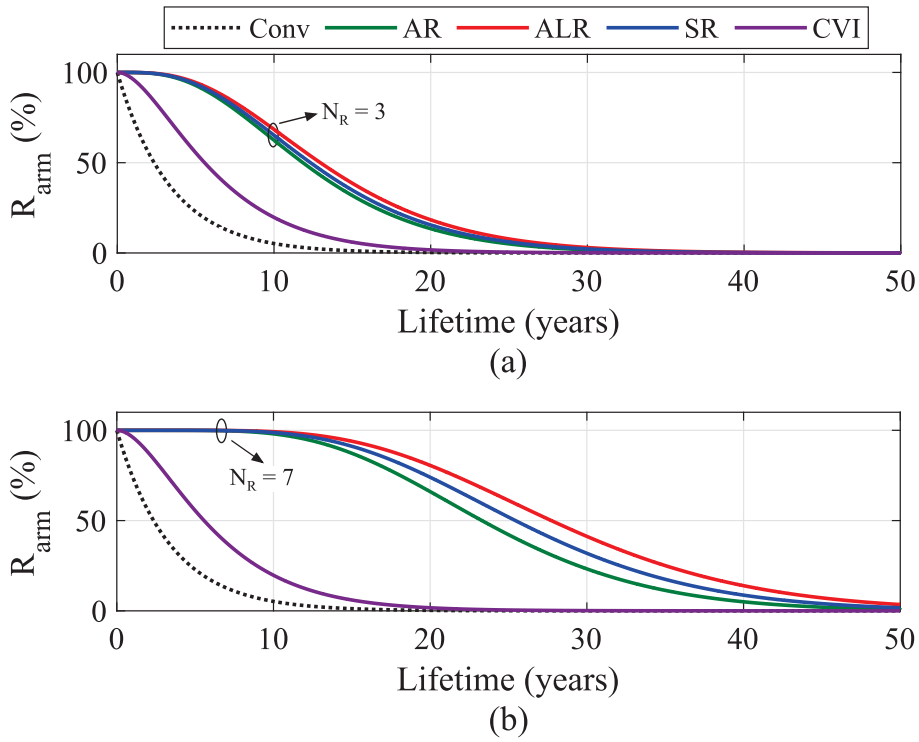
Figure 76 presents the MMC-level reliability for different MMC fault-tolerance schemes. As observed, the conventional approach gives a converter reliability less than 1% for all cases within the target lifetime of 10 years. Moreover, the CVI method improves the reliability for both C_{17} and C_{33} cases, since the voltage ratio can be increased until the safe limits, as observed in Figs. 76 (a) and (b), respectively. Although an improvement in reliability could be observed, the levels are below 1% and 4%, respectively.

Figure 74 – Probabilities of all success states for the solution based on the design C_{17} considering the ALR method. *Remark:* $N_R = 3$.



Source: Elaborated by the author.

Figure 75 – Arm-level reliability function for different fault-tolerant methods based on the design C_{17} considering: (a) $N_R = 3$; (b) $N_R = 7$.



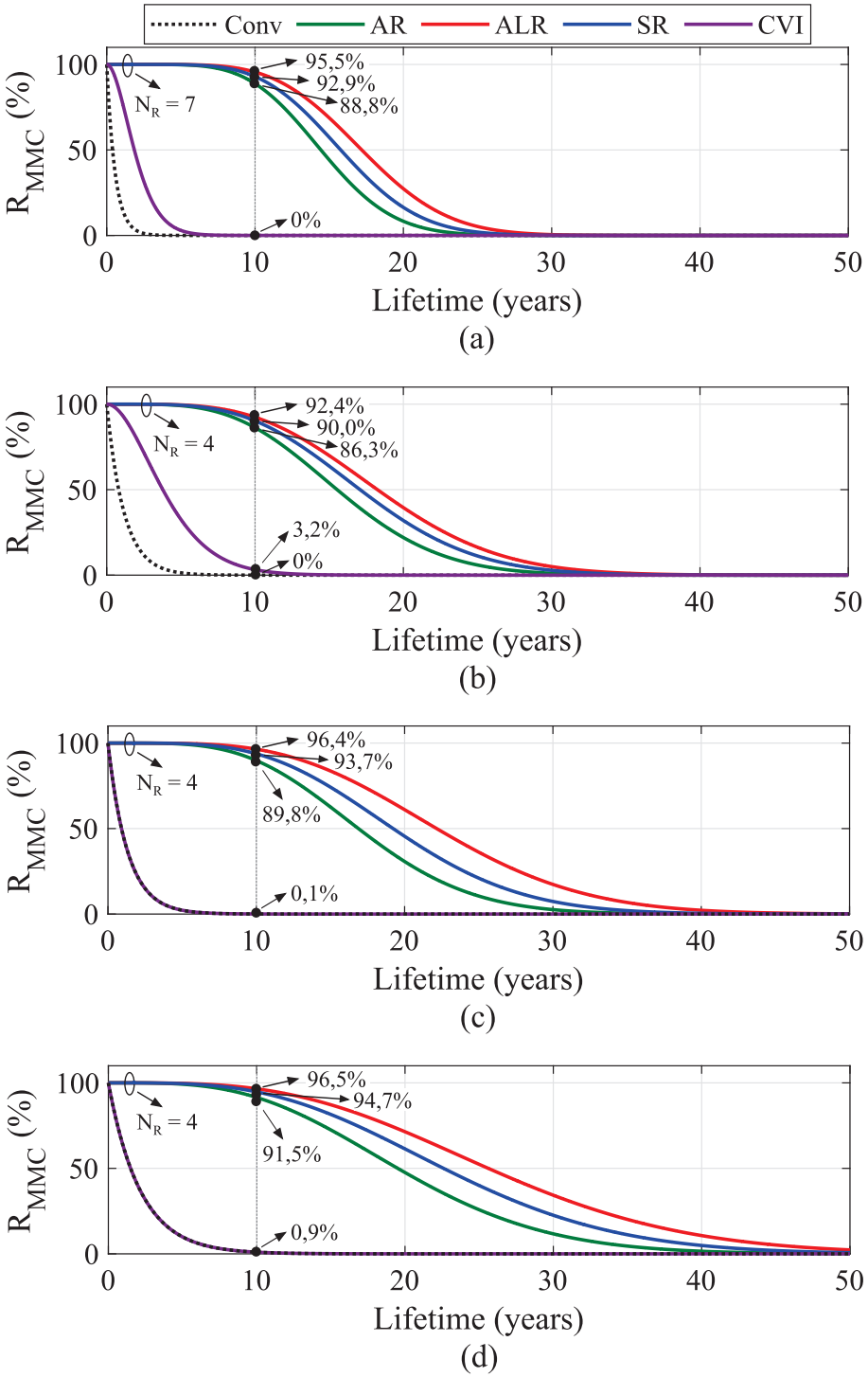
Source: Elaborated by the author.

Regarding redundancy-based methods, the MMC-level reliability is improved according to the increment of redundant SMs. B_{10} approach is considered, which all solutions must be present $R_{MMC}(10\text{years}) \geq 90\%$. Under such conditions, $N_R = 7$ SMs are adopted for C_{17}, and $N_R = 4$ SMs are employed for the other cases. It is important to remark that the cases with more non-redundant SMs require more redundant SMs to achieve high reliability levels. Furthermore, the ALR scheme presents the highest MMC-level reliability, followed by SR and AR methods, respectively.

Figure 77 presents the *reliability vs cost* map of all MMC solutions for different fault-tolerant methods considering a lifetime target of 10 years. Aiming to exemplify the reliability-oriented design, two examples are considered, $R_{MMC}(10\text{years}) \geq 90\%$ and $R_{MMC}(10\text{years}) \geq 99\%$, which are related to the B_{10} and B_1 approaches, respectively. The base value of the cost is 2.27 M€, which refers to the C_{17} design under the conventional approach. As noted, the increase in the number of redundant SMs can cause dispensable CAPEX and OPEX, since the improvement in reliability becomes negligible. Moreover, redundant SMs are unable to improve MMC-level reliability if neglected MMC-level components (e.g., control and protection systems) have predominant failure rates. Under such conditions, redundant MMC-level components must be considered.

As illustrated in Fig. 77, the solutions close to the trend line have the best cost-benefit ratios. Therefore, the solutions based on the design C_{17} stand out as the

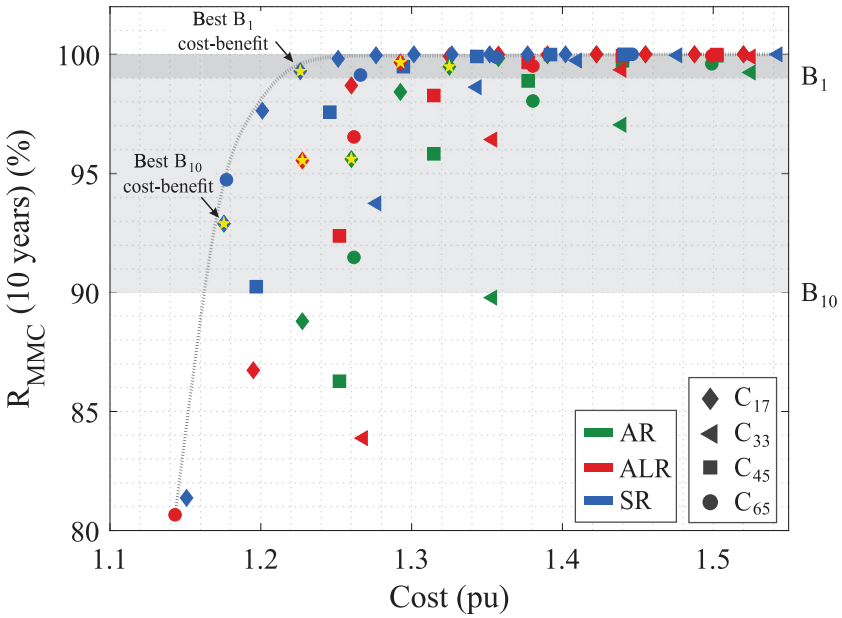
Figure 76 – MMC-level reliability function for different fault-tolerant methods based on the design: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.



Source: Elaborated by the author.

best choices for all fault-tolerance methods presented. A similar result have been found in (Huber; Kolar, 2017) for an 1 MVA CHB. Moreover, the best B_{10} cost-benefit is a solution based on SR method with $N_R = 7$, which present $R_{MMC}(10\text{years}) = 92.9\%$ at the cost of 2.67 M€. Regarding the best B_{10} cost-benefit, the solution based on SR method

Figure 77 – *Reliability vs cost* map of all MMC solutions for different fault-tolerant methods considering a lifetime target of 10 years. *Remark:* the best trade-off for each fault-tolerance method is highlighted considering both B_{10} and B_1 approaches.



Source: Elaborated by the author.

with $N_R = 9$ presents $R_{MMC}(10\text{years}) = 99.3\%$ at the cost of 2.78 M€. It is important to remark that the SR method present the lowest cost, since the cost of extra power supplies for each SM is neglected in the CAPEX of this work.

Table 15 summarizes the best cost-benefit for each fault-tolerant method considering both B_{10} and B_1 approaches, as highlighted in Fig. 77. As observed, the solutions based on SR method present the best features, except for the MMC-level reliability. In this sense, the AR and ALR methods present 95.6% and 99.7% for B_{10} and B_1 approaches, respectively. In addition, the solutions based on AR method need more redundant SMs to achieve the desired MMC-level reliability. It is important to note that according to the

Table 15 – Comparison of the best cost-benefit for each fault-tolerant method highlighted in the *Reliability vs cost* map considering both B_{10} and B_1 approaches.

Parameters	B_{10} **approach**			B_1 **approach**		
	AR	**ALR**	**SR**	**AR**	**ALR**	**SR**
N_R	8	7	7	10	9	9
E_c (MWh)	564	549	442	595	580	442
OPEX (M€)	0.62	0.60	0.49	0.65	0.64	0.49
CAPEX (M€)	2.24	2.19	2.19	2.36	2.30	2.30
Cost (M€)	2.86	2.79	2.67	3.01	2.94	2.78
R_{MMC} (10years) (%)	95.6	95.5	92.9	99.5	99.7	99.3

B_{10} and B_1 approaches, the MMC-level reliability only needs to be greater than 90% and 99%, respectively. Under such conditions, the solutions based on SR method have suitable MMC-level reliability at the lowest cost, since such solutions have lower OPEX.

5.7 Conclusions

This work proposed a reliability-oriented design methodology for MMC-based STATCOM. The MMC-level reliability considering different fault-tolerance schemes is derived using Markov chains and the iteration method. The proposed methodology allows the design engineer to select the most suitable MMC solution according to the trade-off between the converter cost and the reliability requirement.

The presented solutions based on four fault-tolerance methods and four commercially available semiconductor blocking voltages were compared in terms of cost and reliability level. Moreover, the effect on MMC reliability considering the sliding-mode observer was evaluated. As a result, the MMC solutions based on the design of 1.7 kV considering SR method is the best cost-benefit solution to achieve both 90% or 99% of reliability level, during the whole target lifetime.

It is important to note that the proposed methodology can be easily extended to other converter topologies, fault-tolerance methods, and different cost evaluation methodologies. Finally, the best cost-benefit solution for different reliability criteria can be evaluated according to the target lifetime.

6 Closure

The present Ph.D thesis have discussed important issues about the modular multilevel converters focusing in STATCOM application. In that way, a reliability-oriented design for MMC-based STATCOM is presented. The proposed methodology allows the design engineer to select the most suitable MMC solution according to the trade-off between the converter cost and the reliability requirement.

6.1 Conclusions

The conclusions of this Ph.D thesis can be divided into three main parts: design of the MMC-based STATCOM, sliding-mode observer applied to MMC-based STATCOM, and reliability-oriented design based on MMC fault-tolerance methods.

6.1.1 Design of the MMC-based STATCOM (Chapter 2)

- The presented MMC-based STATCOM design stands out suitable for the dynamic responses analyzed: MMC energization, and positive and negative sequences injection.
- The control tuning and strategy adopted shows satisfactory response in terms of reactive power, grid current, circulating current and SM capacitor voltage balancing, which are validate by both experimental and simulation results.
- The energy requirements calculated for the SM capacitors were sufficient to satisfy a 10 % ripple for the analyzes employed.
- The choice of the semiconductors devices were validated in the thermal and power losses analyzes in this work.

6.1.2 Sliding-Mode Observer Applied to MMC-based STATCOM (Chapter 3)

- The MMC based on sliding-mode observer shows satisfactory response for the dynamic responses analyzed: MMC energization, and positive and negative sequences injection. The relative error between the measured and estimated SM capacitor voltage is within $\pm$ 5 % in steady-state for all employed operating conditions.
- A proposed linear corrector within the hysteresis band reduced the chattering in the observer dynamics. The relative error between the measured and estimated SM

capacitor voltage is reduced from ± 4.2 % to ± 2.7 %, when the linear corrector is considered.

- The increased spreading effect at low-switching frequencies is not caused by the adopted sliding-mode observer. Indeed, the spreading in capacitor voltages at low-switching frequencies is an expected effect in MMC.
- The observer gain employed was obtained empirically considering the calculated lower bound value. Low gain values can cause instability in the MMC, as high values cause unnecessary oscillations in the estimated SM capacitor voltages.

6.1.3 Reliability-Oriented Design Based on Fault Tolerance (Chapters 4 and 5)

- The AR strategy presents the best performance in terms of MMC dynamic behavior. Furthermore, the SR strategy results in the worst performance for MMC dynamic behavior, since the charging process of the spare SMs affects the remaining SMs.
- When the rated blocking voltage of the HiPak power devices increases, the switching losses increase. Additionally, total diode conduction losses increase when the blocking voltage is higher, whereas this relationship is not straightforward for IGBTs.
- Solutions based on power devices with higher blocking voltage presented higher reliability level. Moreover, the MMC-level reliability is improved assuming the sliding-mode observer, since the SM capacitor voltage measurements are neglected.
- A fault-tolerance method can be added to improve the converter reliability. There is a minimum limit of redundant SMs to achieve a reliability level $R(t_0)$ for a defined target lifetime t_0. Nevertheless, the increase in the number of redundant SMs can cause dispensable CAPEX and OPEX.
- The proposed *reliability vs cost* map allows the design engineer to select the most suitable MMC solution according to the trade-off between the converter cost and the reliability requirement. In the proposed case study, the MMC solutions based on the design of 1.7 kV considering SR method is the best cost-benefit solution to achieve both 90% or 99% of reliability level, during the target lifetime of 10 years.

6.2 Research Perspectives

While the present Ph.D. thesis has explored and documented numerous aspects, there remains room for further enhancements and future research. From the author's perspective, the following topics could be considered for future work:

- Reliability methodology that combines both random and wear-out failures for the converter components considering different fault-tolerance methods.
- Employment of the reliability methodology to compare solutions based on other technologies of power semiconductor devices, capacitors, etc.
- Evaluate the presented sliding-mode observer for other cascaded multilevel converter topologies, such as CHB.
- Experimental validation of the MMC-LVRT capability and other converter fault-tolerance methods as well.

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APPENDIX A – Appendix

A.1 MMC Control Tuning

A.1.1 Output Current Control

Applying the transformation from abc frame into the stationary ($\alpha\beta$) reference frame in Eq. (2.5), the dynamics of the grid current is given by:

$$v_{s,\alpha\beta} = v_{g,\alpha\beta} - L_{eq}\frac{di_{g,\alpha\beta}}{dt} - R_{eq}i_{g,\alpha\beta}, \tag{A.1}$$

where $L_{eq} = L_g + 0.5L_{arm}$, $R_{eq} = R_g + 0.5R_{arm}$ and $v_{s,\alpha\beta}$ is the equivalent output voltage of the MMC. L_{arm} and R_{arm} are the inductance and the resistance of the arm inductors, respectively.

Furthermore, the block diagram of the output current control is shown in Fig. 78. The PR controller $C_G(s)$ is given by:

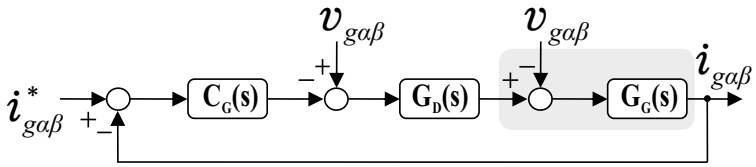

Figure 78 – Block diagram of the output current control.

$$C_G(s) = k_{p,g} + \frac{k_{r,g}}{s^2 + w_g^2}, \tag{A.2}$$

where $k_{p,g}$ is the proportional gain and $k_{r,g}$ the resonant gain of the output current controller that is tuned to the fundamental frequency.

The control system of an MMC is invariably implemented digitally, generally using digital signal processors (DSPs), often combined with field-programmable gate arrays (FPGAs). In such a control system there are some time delays due to factors such as computation, communication, analog-to-digital conversion process that give the computational time delay typically in the same order of magnitude as the sampling period T_s (Sharifabadi et al., 2016). Moreover, the PWM results in a switching time delay of $0.5T_s$. Therefore, the total time delay is the sum of these two components $T_d = 1.5T_s$. Under such conditions, the effect of the implementation delay and the zero-order hold can be represented by the following transfer function:

$$G_D(s) = \frac{1}{sT_d + 1}, \tag{A.3}$$

Furthermore, the plant transfer function of output current can be described by:

$$G_G(s) = \frac{1}{sL_{eq} + R_{eq}}, \tag{A.4}$$

According to Sharifabadi et al. (2016), the objective is to maximize the current control bandwidth. Thus, the PR gains can be obtained by:

$$k_{p,g} = 2\pi f_{c,g} L_{eq}, \tag{A.5}$$

$$k_{r,g} = 2\pi f_{h,g} k_{p,g}, \tag{A.6}$$

where $f_{c,g}$ is the desired closed-loop-system bandwidth and $f_{h,g}$ is the resonant part bandwidth.

As noted, the total time delay is not generally negligible. Under such conditions, there is an upper limit for $f_{c,g}$ that must be observed for the closed-loop system to remain stable with large enough margins. An useful rule of thumb is:

$$f_{c,g} \leq \frac{f_s}{10}, \tag{A.7}$$

Moreover, $f_{h,g}$ should attend the follow conditions:

$$f_{h,g} \ll f_{c,g}, \tag{A.8}$$

$$f_{h,g} \leq f_g, \tag{A.9}$$

A.1.2 Global Energy Control

The block diagram of the global energy control is illustrated in Fig. 79.

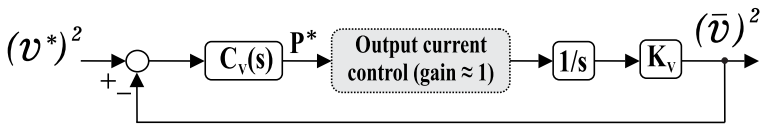

Figure 79 – Block diagram of the global energy control.

Assuming an evenly distribution of the energy among the converter SMs and neglecting the converter losses, the behavior of the SM capacitor voltage can be represented by the total energy storage:

$$W_T = \sum_{n=1}^{6N} \frac{1}{2} C v_n^2 = 3CN\, V^{*\,2}\,, \tag{A.10}$$

The time derivative of (A.10) represents the instantaneous power stored in the SM capacitors. Thus, $V^{*\,2}\,(s)$ can be described by:

$$V^{*\,2}\,(s) = \frac{PK_V}{s}, \tag{A.11}$$

where K_V is given by:

$$K_V = \frac{1}{3CN}. \tag{A.12}$$

Considering the ideal output current control loop, the outer open-loop transfer function is obtained by:

$$G_V(s) = C_V(s)\frac{1}{3CNs}, \tag{A.13}$$

where $C_V(s)$ is a PI controller, given by:

$$C_V(s) = \left(k_{p,v} + \frac{k_{i,v}}{s}\right). \tag{A.14}$$

The tuning of the controllers is carried out by the pole allocation method. According the methodology discussed in Sousa (2011), the gains for the poles of the transfer function in closed-loop to be real and allocated in the left semiplane, can be obtained as follows:

$$\begin{aligned} k_{p,v} &= \frac{2\pi\,(f_{v1} + f_{v2})}{K_V}, \\ k_{i,v} &= \frac{4\pi^2 f_{v1} f_{v2}}{K_V}, \end{aligned} \tag{A.15}$$

where f_{v1} and f_{v2} are the poles of the closed-loop transfer function. Typically, these poles are separated by a decade and the value of the largest of them must be allocated, at least, one decade below the cutoff frequency of the current grid. This guarantees the proper operation of the cascade control. Therefore, these frequencies can be defined as:

$$f_{v1} \leq \frac{f_{c,g}}{10}, \tag{A.16}$$

$$f_{v2} \leq \frac{f_{v1}}{10}. \tag{A.17}$$

A.1.3 Circulating Current Control

The circulating-current dynamics are governed by (2.7) as:

$$\frac{v_{dc}}{2} - v_c = L_{arm}\frac{di_c}{dt} + R_{arm}i_c, \tag{A.18}$$

Therefore, a feedforward term, $\frac{v_{dc}}{2} - R_{arm}i_c$ (where, in practice, an estimate must be used in place of R_{arm}), can be added to compensate the resistive voltage drop and term $\frac{v_{dc}}{2}$ in (A.18). Therefore, the following control law is obtained:

$$v_c^* = \frac{v_{dc}}{2} - (i_c^* - i_c)C_c(s) - R_{arm}i_c^*, \tag{A.19}$$

where $C_C(s)$ is the PR controller given by:

$$C_C(s) = k_{p,c} + \frac{k_{r,c}}{s^2 + (2\omega_g)^2} + \frac{k_{r,c}}{s^2 + (4\omega_g)^2}, \tag{A.20}$$

where $k_{p,c}$ is the proportional gain and $k_{r,c}$ is the resonant gain of the circulating current controller. A considerable 2nd harmonic component is present in the circulating current. This second order component generally cannot be compensated by the proportional controller. In view of this problem, the resonant controller is tuned to the second- and fourth-order harmonic frequencies.

The block diagram of the circulating current control is shown in Fig. 80. Since $v_c \approx \frac{v_{dc}}{2}$, i.e. the feedforward term dominates and the contribution from the PR controller is small, saturation and anti-windup schemes need not be applied in this loop (Sharifabadi et al., 2016).

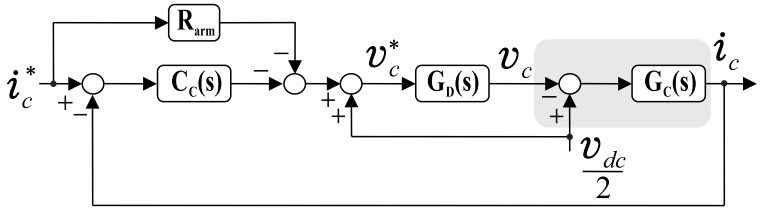

Figure 80 – Block diagram of the individual voltage balancing control.

As noted, v_c is equals a v_c^* delayed T_d, which is given by $v_c = e^{-sT_d}v_c^*$. Moreover, the plant transfer function $G_C(s)$ of circulating current can be represented by:

$$G_C(s) = \frac{1}{sL_{arm} + R_{arm}}, \tag{A.21}$$

The PR gains are obtained analogously to the gains of the inner loop of output current control. Therefore, the PR gains can be obtained by (Sharifabadi et al., 2016):

$$k_{p,c} = 2\pi f_{c,c} L_{arm}, \tag{A.22}$$

$$k_{r,c} = 2\pi f_{h,c} k_{p,c}, \tag{A.23}$$

where $f_{c,c}$ is the desired closed-loop-system bandwidth and $f_{h,c}$ is the resonant part bandwidth. $f_{c,c}$ and $f_{h,c}$ conditions are:

$$f_{c,c} \leq \frac{f_s}{10}, \tag{A.24}$$

$$f_{h,c} \ll f_{c,c}, \tag{A.25}$$

$$f_{h,c} \leq f_g, \tag{A.26}$$

A.1.4 Individual Voltage Balancing Control

The block diagram of the individual voltage balancing control is presented in Fig 81 (Maharjan; Inoue; Akagi, 2008). For the sake of simplicity, only upper arm of phase A is considered. In this case, K_B is given by:

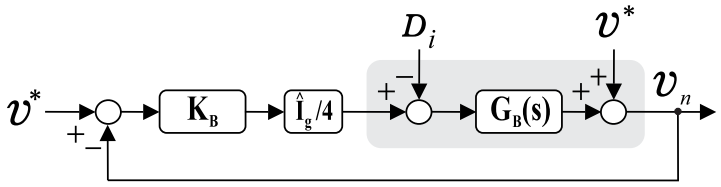

Figure 81 – Block diagram of the circulating current control.

The goal of this control is to keep each of the three dc voltages in an arm equal to the dc mean voltage of the corresponding arm (Maharjan; Inoue; Akagi, 2008). The difference between the reference voltage and the dc voltage of the n-th converter SM (v_n) is given by:

$$\Delta v_n = v^* - v_n. \tag{A.27}$$

The compensating voltage to minimize Δv_n can be expressed as (Maharjan; Inoue; Akagi, 2008):

$$v_b = k_{p,b} \Delta v_n \sin(\omega_g t). \tag{A.28}$$

Equation (A.28) means that the individual balancing controller has a proportional gain of $k_{p,b}$:

$$K_B = k_{p,b}. \tag{A.29}$$

Moreover, considering STATCOM operation, the upper arm current can be expressed by:

$$i_u = \frac{\widehat{I}_g}{2}\sin(\omega_g t). \tag{A.30}$$

The active power for dc-voltage balancing of the nth SM capacitor can be written as:

$$p_b = v_b i_u - D_i, \tag{A.31}$$

where D_i represents the losses or disturbance in the nth SM capacitor. Replacing (A.28) and (A.30) into (A.31), the follow equation is obtained:

$$p_b = \frac{k_{p,b}\Delta v_n \widehat{I}_g}{4}[1-\cos(2\omega_g t)] - D_i. \tag{A.32}$$

Thus, Δv_n can be expressed by:

$$\Delta v_n \approx -\frac{1}{C}\int \frac{p_b}{V^*}dt. \tag{A.33}$$

From the diagram block of Fig. 81, the closed-loop transfer function is given by:

$$\frac{\Delta V_n(s)}{D_i(s)} = \frac{1}{\underbrace{sCV^*}_{G_B(s)} + \frac{\hat{I}_g}{4}k_{p,b}}. \tag{A.34}$$

Furthermore, the closed-loop poles must be located in the left semiplane for the system to be stable. Therefore, the proportional gain can be calculated as follows:

$$k_{p,b} = \frac{8\pi f_{c,b} CV^*}{\hat{I}_g}, \tag{A.35}$$

where fc, b is the location of the closed-loop pole. The frequency of the individual balancing control are defined to attend closed-loop-system bandwidth lower than all other controllers. Thus, the frequency can be given by:

$$f_{c,b} \leq \frac{f_s}{10^3}. \tag{A.36}$$